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DESIGN AND IMPLEMENTATION OF INTEGRATED HIGH EFFICIENCY  
LOW-VOLTAGE CMOS DC-DC CONVERTERS

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Ce mémoire intitulé :

DESIGN AND IMPLEMENTATION OF INTEGRATED HIGH EFFICIENCY  
LOW-VOLTAGE CMOS DC-DC CONVERTERS

présenté par : M. AL-TERKAWI HASIB Omar

en vue de l'obtention du diplôme de : Maîtrise ès Sciences Appliquées

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*To my dear mother,  
I can't be grateful enough. . .*

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# Résumé

De nos jours, les appareils portatifs sont utilisés dans plusieurs applications. Ils utilisent en général une batterie qui doit être remplacée ou rechargée régulièrement. Dans le cas d'applications biomédicales, la durée de vie de la batterie est un paramètre critique. Pour un appareil implantable, une longue durée de vie est un objectif primordial. Cet objectif est généralement atteint en réduisant la consommation de puissance des circuits constituant l'implant. Parmi les diverses techniques existantes qui permettent la réduction de la consommation en puissance des circuits CMOS, on retrouve la technique d'ajustement dynamique de la tension (dynamic voltage scaling - DVS). En réduisant la tension d'alimentation, la consommation totale des circuits peut être diminuée. Cependant cette technique ne peut être implémentée sans faire appel à des circuits dédiés à une gestion intelligente de l'énergie. Dans ce contexte, l'utilisation de convertisseurs de tension DC-DC devient nécessaire pour économiser la charge de la batterie. Mais pour garantir une réduction effective de la consommation globale, des convertisseurs DC-DC de haute efficacité doivent être utilisés. A cette contrainte se rajoute la miniaturisation en utilisant des circuits hautement intégrés pour les applications telles que les implants biomédicaux. Le défi réside dans la conception d'un convertisseur DC-DC totalement intégré tout en assurant une haute efficacité sur une grande plage de tension de sortie. De plus, les appareils tels que les implants électroniques fonctionnent souvent en mode de veille pour réduire la consommation, entraînant ainsi des variations conséquentes de la charge du convertisseur DC-DC. Ceci rajoute un défi supplémentaire pour le maintien d'une haute efficacité de la conversion DC-DC à faible charge.

Dans ce mémoire, nous présentons la conception détaillée d'un convertisseur DC-DC hautement efficace et totalement intégré dans une technologie CMOS à faible tension. Nous proposons une implémentation originale et totalement intégrée d'un convertisseur DC-DC à capacités commutés (switched capacitor - SC) opérant avec un contrôle asynchrone. L'efficacité du convertisseur est maintenue élevée en ajustant sa topologie et sa fréquence d'opération selon la charge. Le convertisseur SC DC-DC proposé utilise trois topologies distinctes pour réaliser trois taux de conversion différents. Ainsi, le convertisseur maintient une haute efficacité à différents niveaux de tensions de sortie. De plus, afin de réduire les pertes d'énergie, le contrôle asynchrone adapte la fréquence d'opération aux diverses conditions de charge. Ce contrôle est également capable d'adapter la taille des interrupteurs du convertisseur SC DC-DC pour améliorer encore plus l'efficacité de la conversion. Les résultats expérimentaux de ce travail confirment la théorie et les simulations conduites lors de la conception. Une puce

de  $1.5 \times 1.5 \text{ mm}^2$  contenant le convertisseur proposé a été fabriqué en utilisant la technologie IBM CMOS  $0.13 \mu\text{m}$ . Le convertisseur est capable d'atteindre une efficacité maximale de 80% en fournissant une tension de sortie entre  $0.3\text{V}$  et  $1.1\text{V}$  à partir d'une entrée à  $1.2\text{V}$ . Le convertisseur utilise un ensemble de condensateurs intégré dont la capacité totale est de  $350\text{pF}$  pour fournir une puissance de sortie maximale de  $230\mu\text{W}$ , ciblant ainsi de nombreuses applications à très faible puissance.



# Abstract

Today, battery-powered portable devices are used in many applications. In applications like biomedical implants, the battery life is a major concern. Since replacing the battery of an implant needs a surgical procedure, a long battery life is a goal that all implants try to achieve. This is normally done by reducing the power dissipation in the implant's circuitry. One of the various techniques that exist for reducing the power consumption in CMOS circuitry is the dynamic voltage scaling (DVS) technique. By reducing the supply voltage, the overall power consumption of the circuits can be decreased. This technique cannot be implemented without power management blocks. The use of DC-DC converters becomes a must to save battery power. The overall power reduction can be improved by introducing high efficiency DC-DC converters. Moreover, to provide patients with the most comfort, small integrated circuits should be used in applications such as biomedical implants.

The challenging aspect of designing integrated DC-DC converters is keeping the efficiency high while providing an adjustable output voltage. Additionally, devices such as electronic implants go in and out of stand-by mode to reduce power consumption. From the perspective of the DC-DC converter, the output load power is varying according to the mode of operation of the implant. This adds another challenge of sustaining the DC-DC conversion efficiency high under various loading conditions. At very light loads, preserving a high conversion efficiency is a challenge.

In this master thesis, a detailed design of a high-efficiency low-voltage fully integrated DC-DC converter is presented. A unique structure of a fully integrated switched-capacitor (SC) DC-DC converter with asynchronous control is proposed. The efficiency of the converter is maintained high by adjusting the converter topology and operating frequency according to the loading conditions. The proposed SC DC-DC converter uses three different topologies to achieve three different conversion ratios. By doing so, the converter maintains high conversion efficiency at various output voltage levels. Also, an adaptive operating frequency is used by the asynchronous control to reduce efficiency losses at various loading conditions. Moreover, the applied control is able to change the size of the switches in the SC DC-DC converter when needed. This leads to further enhancement in the overall conversion efficiency. The simulations and experimental results of this work supported the theories of the design. The converter was fabricated on a  $1.5 \times 1.5\text{mm}^2$  chip using IBM CMOS  $0.13\mu\text{m}$  technology. Operating with an input voltage of  $1.2\text{V}$ , the proposed DC-DC converter is able to provide

output voltages between  $1.1V$  and  $0.3V$  with a maximum efficiency of 80%. This design is aimed at ultra-low-power applications. It uses a total of  $350pF$  on-chip capacitors to support a maximum output power of  $230\mu W$ .

# Condensé en français

## 1. Introduction

Au cours de la dernière décennie, la demande d'appareils portatifs a connu une augmentation constante. Grâce à la miniaturisation, aux multiples fonctionnalités et à la possibilité de les alimenter par batterie uniquement, ces appareils ont trouvé leur place dans de nombreuses applications y compris les implants biomédicaux. Dans de tels systèmes, la durée de vie de la batterie est un facteur crucial [35]. Il est donc nécessaire d'augmenter la durée de vie de la batterie et cela passe par la réduction autant que possible de la dissipation de puissance des composants électroniques.

L'ajustement dynamique de la tension (DVS) constitue la principale technique utilisée pour réduire la consommation d'énergie des circuits CMOS [47]. Celle-ci exploite le fait que la consommation d'énergie est reliée de manière quadratique à la tension d'alimentation (équation 1.1). Pour tirer avantage de la technique DVS, des convertisseurs DC-DC abaisseurs de tension qui peuvent fournir des sorties variables sont requis [10, 19, 26, 29, 30, 40]. De plus, il a été démontré que la technique DVS utilisée dans un système asynchrone peut réduire encore plus la consommation de puissance des circuits utilisés [24].

L'objectif de ce travail est de concevoir un convertisseur DC-DC hautement efficace, totalement intégré et dédié aux implants biomédicaux. Le type de convertisseur DC-DC proposé est à capacités commutées (switched capacitor- SC) avec un taux de conversion variable. Ce type de convertisseurs convient aux implants biomédicaux car il est efficace et peut être complètement intégré sur puce [29, 43]. Pour être capable d'appliquer la technique DVS, le convertisseur SC DC-DC doit varier la tension de sortie. Cependant, l'efficacité de conversion maximale que le convertisseur SC DC-DC puisse fournir dépend de la tension de sortie (équation 2.5). Heureusement, ce problème peut être résolu en ajustant le taux de conversion du SC DC-DC en fonction de la tension de sortie requise. Il existe différents types de pertes d'énergie qui contribuent à la réduction de l'efficacité (équation 2.8). L'une des principales pertes d'énergie est due aux commutations ( $E_{sw}$ ). Ces pertes dépendent de la fréquence de commutation. Afin de réduire ces pertes, le convertisseur SC DC-DC devrait commuter seulement quand c'est nécessaire. Or, un convertisseur SC DC-DC dépend en général d'une fréquence d'horloge constante. La puissance de sortie, l'efficacité de la conversion ainsi que le choix de la taille des condensateurs et des commutateurs au moment de la conception

dépendent de la fréquence de cette horloge.

La recherche d'une fréquence d'opération optimale qui maximiserait l'efficacité par rapport à la taille des condensateurs et des commutateurs peut être laborieuse. Ceci devient encore plus complexe quand le convertisseur SC utilise différentes topologies à différentes tensions de sortie. La conception présentée ici utilise un contrôleur totalement asynchrone qui varie la fréquence selon la topologie utilisée et selon le courant requis par la charge du convertisseur DC-DC. Le contrôleur réduit la commutation au minimum nécessaire et réduit ainsi les pertes de puissance associées à la commutation. De plus, afin de pouvoir opérer sur une large plage de tension de sortie tout en maintenant une bonne efficacité, le convertisseur SC DC-DC proposé bascule entre trois différentes topologies permettant les taux de conversions suivants :  $1, \frac{2}{3}$  et  $\frac{1}{3}$ .

## 2. Conception du convertisseur SC DC-DC proposé

### 2.1 Vue d'ensemble de la structure proposée

Un aperçu complet de la structure proposée est illustré à la Fig. 3.1. Le réseau du convertisseur (SC DC-DC converters network) a la possibilité de changer sa topologie en fonction des signaux numériques  $T_1$  et  $T_2$ . Les taux de conversion qui peuvent être réalisés par les topologies possibles sont  $1, \frac{2}{3}$  et  $\frac{1}{3}$ . La quatrième combinaison de  $T_1$  et  $T_2$  désactive le convertisseur. La boucle de rétroaction est constituée d'un comparateur à deux tensions de seuil, d'un contrôleur asynchrone (Asynchronous Controller), d'un détecteur de mode (Mode Detector) et d'un sélecteur de mode (Mode Selector). Le comparateur génère deux signaux numériques,  $V_A$  et  $V_B$ .  $V_A$  est le résultat de la comparaison entre  $V_{out}$  et  $V_{aim}$ , alors que  $V_B$  est généré par un seuil inférieur à  $V_{aim}$  de près de 0.1V. La combinaison de  $V_A$  et de  $V_B$  crée trois valeurs d'entrée possibles utilisées par le contrôleur asynchrone.

Le contrôleur asynchrone proposé génère trois signaux dont les largeurs d'impulsion et les fréquences sont ajustées en fonction de la charge. Ces signaux de commande sont transmis au réseau du convertisseur SC DC-DC par l'intermédiaire du sélecteur de mode, qui choisit entre deux modes d'opération : soit le mode asynchrone (Asynchronous Drive Mode) qui est le principal mode de fonctionnement, soit le mode synchrone (Synchronous Drive Mode) qui est un mode de repli disponible lorsque la charge dépasse la valeur attendue. En mode asynchrone, les signaux du contrôleur sont transmis au réseau du convertisseurs SC DC-DC, tandis que dans le mode synchrone, les signaux sont transmis à partir d'un générateur d'horloge.

Le sélecteur de mode choisit un signal pour piloter le réseau du convertisseurs en se basant sur le signal "Decision" issu du détecteur de mode. Pour des valeurs de charge régulières, le signal Decision est au niveau bas, ce qui désactive le générateur d'horloge et transmet les signaux du contrôleur asynchrone vers le réseau du convertisseurs SC DC-DC. Quand la charge de courant dépasse la capacité nominale du réseau de convertisseurs, le signal Decision passe au niveau haut et configure le convertisseur à un circuit synchrone en activant une horloge à 4 MHz pour opérer le convertisseur. La raison principale pour basculer vers le mode synchrone est de maintenir l'ondulation de la tension de sortie faible dans le cas de grands courants de charge. Ceci sera expliqué dans la section suivante.

Selon la taille des condensateurs et des commutateurs utilisés ainsi que la topologie choisie, il y a une limite de courant qui peut être délivré à la charge. Le détecteur de mode est le bloc qui détecte quand la limite de courant du réseau de convertisseurs est dépassée. Le processus de détection se fait par l'inspection du motif des signaux générés par le contrôleur asynchrone. Une fois que le motif régulier change, le détecteur de mode envoie le signal "Support" au réseau de convertisseurs. Ce signal active des commutateurs supplémentaires parallèles dans le convertisseur. Ce faisant, le convertisseur augmente la limite maximale du courant de charge d'une certaine valeur. Si cela s'avère insuffisant pour alimenter la charge, alors le détecteur passe le signal Decision au niveau haut mettant ainsi le convertisseur en mode synchrone.

## 2.2 Stratégie de contrôle asynchrone

Le réseau de convertisseurs dans la structure présentée précédemment est constitué d'un commutateur direct et de deux convertisseurs SC DC-DC à topologie ajustable (Fig. 3.2). Le commutateur direct est utilisé pour initialiser la capacité de charge à la tension désirée, et les convertisseurs SC DC-DC gardent  $V_{out}$  à cette valeur. Cette opération donne au convertisseur non seulement un temps de montée rapide lors du basculement entre les topologies mais également une conversion efficace en régime permanent. Chacun des convertisseurs SC DC-DC est composé de trois condensateurs et de onze interrupteurs (Fig. 3.3). Selon les topologies utilisées, les interrupteurs sont réglés sur ON ou OFF, sous contrôle d'un signal ou de son complément (voir le tableau 4.3). L'arrangement illustré dans la Fig. 3.3 peut connecter les condensateurs dans quatre différentes combinaisons série-parallèle qui permettent trois taux de conversion possibles ( $1$ ,  $\frac{2}{3}$  et  $\frac{1}{3}$ ).

Le contrôleur asynchrone est en réalité une machine à états asynchrone. Pour piloter le réseau de convertisseurs SC DC-DC de manière asynchrone, le contrôleur attend certains

événements qui sont déclenchés par la tension de sortie. Ces événements sont détectés par le comparateur qui compare  $V_{out}$  à deux seuils  $V_{Aref}$  et  $V_{Bref}$ . Dans le circuit proposé,  $V_{Aref} = V_{aim}$ ,  $V_{Bref} = V_{aim} - 0.1V$  et  $V_{aim}$  est la tension de sortie désirée. De ces deux seuils,  $V_A$  et  $V_B$  sont générés par le comparateur. Le diagramme d'états qui définit la génération des signaux de contrôle  $S_0$ ,  $S_1$  et  $S_2$  par rapport à  $V_A$  et  $V_B$  est montré dans la Fig. 3.6. Le circuit complet du contrôleur asynchrone est donné sur la Fig. 4.2.

Lorsque le circuit démarre pour la première fois, le contrôleur détecte que  $V_{out}$  est inférieur aux deux seuils puis fournit les signaux de commande de manière à ce que la capacité de charge ainsi que les deux convertisseurs SC commencent à se charger. Aussitôt que la tension de sortie dépasse  $V_{Aref}$ , le contrôleur désactive le commutateur direct. La différence entre la constante de temps du mécanisme de charge RC et le retard dans la boucle de rétroaction entraîne des dépassements de tension de sortie. Ensuite, le contrôleur va attendre que la tension de sortie descende en dessous de  $V_{Aref}$  pour connecter l'un des convertisseurs SC à la charge. Dans des conditions normales de charge, la charge stockée par le convertisseur va relever la tension au delà de  $V_{Aref}$ . Le convertisseur connecté fournira la tension de sortie nécessaire jusqu'à ce que toutes les charges disponibles soient consommées. Lorsque la tension de sortie redescend en dessous de  $V_{Aref}$ , le contrôleur connecte la sortie à l'autre convertisseur SC pendant que le précédent se recharge. A partir de là, le contrôleur continuera d'alterner les deux convertisseurs pour alimenter la charge. La Fig. 3.5(a) montre un chronogramme qui résume cette opération de contrôle en fonction de la tension de sortie.

Quand la charge devient supérieure à la valeur attendue, le convertisseur SC DC-DC ne sera pas en mesure d'élever  $V_{out}$  au dessus de  $V_{Aref}$  avant que la charge stockée soit consommée. La tension  $V_{out}$  commencera alors à baisser jusqu'à ce qu'elle atteigne  $V_{Bref}$  (Fig. 3.5(b)). À ce moment là, le contrôleur asynchrone activera l'interrupteur direct pour élever la tension de sortie. Cela remettra à zéro l'opération du contrôleur et ce dernier essaiera de soutenir la charge de nouveau avec les convertisseurs. Si la charge reste élevée pendant un certain temps, le détecteur de mode activera des interrupteurs de sortie additionnels. Dans le cas où cela ne résoud pas le problème, le détecteur de mode décidera de passer au mode synchrone pour parvenir à une meilleure régulation.

## 2.3 Détecteur de Mode et Sélecteur de Mode

Le bloc qui est chargé de déterminer si les convertisseurs SC sont en mesure de supporter la charge ou pas, est le détecteur de mode. Il peut indirectement déterminer si le courant de charge dépasse les capacités des convertisseurs SC en inspectant le motif du signal de

commande générée par le contrôleur asynchrone. Comme vu précédemment sur la Fig. 3.5(b), le motif des signaux de commande  $S_0$ ,  $S_1$  et  $S_2$  change quand le convertisseur SC ne peut pas supporter la charge.

Le détecteur de mode illustré sur la Fig. 3.7 est conçu pour détecter ce motif. Initialement, le détecteur de mode est remis à zéro. Cela implique que toutes les bascules du circuit sont remises à zéro et les signaux Support et Decision sont au niveau bas. Quand le détecteur de mode est activé, il désactivera tous les transistors de remise à zéro et activera  $M_2$ ,  $M_7$ ,  $M_{11}$  et  $M_{16}$ . Le motif normal débutera avec le passage à '1' de  $S_1$  alors que  $S_0$  et  $S_2$  sont à '0'.  $S_1$  activera le transistor  $M_3$  qui tire le courant de cette branche et bascule l'état de *Latch1* pour appliquer finalement un niveau haut sur la grille de  $M_9$ .

Maintenant  $M_9$  est activé et il y a deux scénarios possibles : soit  $S_2$  passe à '1' alors que  $S_1$  passe à '0' (cas normal), soit  $S_0$  passe à '1' et  $S_1$  passe à '0' (si le courant de charge a dépassé la limite). Dans le premier cas,  $M_5$  sera activé et remettra *Latch1* à son état initial qui désactive  $M_9$ . Alors que  $S_1$  et  $S_2$  s'alternent, *Latch1* continuera à changer d'état et le signal Support restera bas. Dans le second cas,  $M_8$  sera activé et basculera l'état de *Latch2*, passant le noeud  $X_1$  au niveau haut. Pour éviter des erreurs dans le processus de détection, les portes NAND couplées par croisement garantiront que  $S_1$  a complètement atteint zéro avant de changer le signal Support à '1'.

Une fois que le signal Support est haut, des commutateurs supplémentaires dans les convertisseurs sont activés pour supporter le courant de charge élevée. Si cela n'était pas suffisant pour supporter la charge, le motif des signaux de commande sera répété. Le bloc B dans le détecteur de mode détectera la répétition du motif et délivrera le signal Decision. Lorsque le signal Decision est haut, le sélecteur de mode va basculer vers le mode synchrone. Fig. 4.4 montre le circuit du sélecteur de mode. La transition entre les deux modes d'opération ainsi que les signaux de commande du contrôleur asynchrone et du détecteur de mode sont montrés dans la Fig. 4.7.

## 2.4 Comparateur à double seuils

Le comparateur qui a été utilisé pour ce convertisseur est montré sur la Fig. 4.5. Pour réduire la consommation d'énergie et la surface de silicium, nous avons conçu un comparateur à deux seuils plutôt que d'utiliser deux comparateurs. Ce comparateur est basé sur un amplificateur opérationnel à transconductance (OTA) et des miroirs de courant. Ceci a été inspiré du travail accompli par [16].

Le comparateur fonctionne comme suit.  $M_8$  est utilisé pour polariser le comparateur. La paire différentielle  $M_6$ - $M_7$  permettra de comparer la tension de sortie  $V_{out}$  du convertisseur DC-DC avec  $V_{ref}$  qui est la tension désirée. Le résultat de la comparaison résultera en un courant dans l'une des branches de la paire différentielle. Le courant est ensuite acheminé à  $M_2$  et  $M_{10}$ . La différence entre les courants de drains de  $M_2$  et  $M_{10}$  va tirer  $V_A^*$  soit vers  $V_{dd}$  ( $1.2V$ ) soit vers la masse. Les transistors  $M_2$  et  $M_{10}$  sont de dimensions telles que  $V_A^* = 0.6$  lorsque  $V_{out} = V_{aim}$ . En changeant la taille des transistors de sortie, le seuil peut être déplacé.  $M_1$  et  $M_9$  sont dimensionnés de sorte que  $V_B^*$  est généré à un seuil inférieur à  $V_A^*$  de  $60mV$ . Pour générer  $V_A$  et  $V_B$  qui déclenchent le contrôleur asynchrone,  $V_A^*$  et  $V_B^*$  sont amplifiés par des inverseurs.

La Fig. 4.6 présente les résultats des analyses de simulation DC du comparateur montré sur la Fig. 4.5. Le balayage est fait avec  $V_{bias} = 0.2V$  et  $V_{aim} = 0.6V$ . Les résultats sur la Fig. 4.6(a) montrent la génération de  $V_A^*$  et  $V_B^*$ . Le seuil supérieur peut être mesuré à  $599.2mV$  alors que le seuil inférieur est de  $541.1mV$ . Quant à la consommation de puissance, ce comparateur ne consomme que  $2.4\mu W$  au maximum qui se produit lorsque  $V_{out} = V_{aim}$ . Fig. 4.6(b) montre le courant dans chaque branche du comparateur, ainsi que le courant total consommé.

### 3. Résultats

La conception présentée dans ce mémoire a été implémentée dans l'environnement Cadence avec la technologie CMOS  $0.13\mu m$  de IBM. La structure complète, excepté le générateur d'horloge, a été intégrée et une puce a été fabriquée. Fig. 3.8 montre une vue microscopique de la puce résultante. La superficie totale incluant les pads est de  $2.225mm^2$  mais seulement  $0.52mm^2$  de cette superficie est effectivement occupée par les circuits actifs. Celle-ci utilise des capacités intégrées MIM de  $150pF$  pour chaque convertisseur, plus  $50pF$  pour le condensateur de sortie. Le courant maximum qui peut être fourni est de  $240\mu A$ . Ceci peut être facilement augmenté en augmentant la taille des condensateurs utilisés. Le convertisseur fonctionne sur une alimentation de  $1.2V$  et peut fournir des tensions de sortie de  $300mV$  à  $1.1V$ .

Les Fig. 3.9 et 4.11 montrent la régulation de la tension de sortie à des valeurs différentes. D'autre part, Fig. 3.10 et 4.8-4.10 montrent l'efficacité du convertisseur sous différentes topologies, différents courants de charge et différentes tensions de sortie. Dans les dernières figures, l'efficacité a été séparée en trois courbes nous permettant de voir la contribution des pertes liées aux composants parasites, celles dues à la commutation et à la conduction.



Les courbes d'efficacité présentée sont définies dans les équations (3.3-3.5). De plus, dans ces figures les courbes d'efficacité avec et sans les pertes de commutation sont presque parallèles, impliquant que celles-ci diminuent quand le courant de charge est réduit. En outre, à faible charge, les pertes dans les composants parasites et les fuites de courant réduisent l'efficacité de manière drastique. Enfin, la comparaison avec les récents travaux effectués sur les convertisseurs SC DC-DC montre que nous avons réussi à obtenir de bons résultats lorsque le convertisseur est commandé de manière asynchrone (tableau 3.1).

## 4. Conclusion

L'importance de la durée de vie de la batterie pour les appareils portatifs et les implants biomédicaux a conduit les chercheurs à développer de nouvelles méthodes de réduction de la consommation de puissance. L'ajustement dynamique de la tension (DVS) est l'une des méthodes les plus connues pour réduire la consommation de puissance des circuits CMOS. Pour appliquer cette technique, des convertisseurs DC-DC à tension de sortie ajustable sont utilisés. À cette fin, nous avons conçu un convertisseur DC-DC qui serait approprié pour de telles applications.

Dans ce mémoire, nous avons conçu et démontré un convertisseur SC DC-DC hautement efficace et totalement intégré dans une structure capable de supporter des systèmes à très faible consommation d'énergie grâce à une tension de sortie ajustable et un fonctionnement asynchrone. Pour ce convertisseur, nous avons adopté une stratégie asynchrone pour minimiser les pertes d'énergie dues à la commutation et les pertes dynamiques des circuits logiques en adaptant la fréquence d'opération aux conditions de charge. En se basant sur la stratégie proposée de commande asynchrone, un processus de détection intelligent a été développé pour ajuster la taille des interrupteurs utilisés selon la puissance de sortie. En outre, un mode de repli synchrone a été incorporé pour rendre le convertisseur robuste en présence de conditions de charge inattendues. Enfin, les théories adoptées et les circuits conçus ont été vérifiés par des mesures expérimentales. Les résultats obtenus s'avèrent compétitifs avec les travaux récents dans ce domaine.

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# List of Abbreviations and Symbols

## Abbreviations:

ADM	Asynchronous Drive Mode.
AFS	Automatic Frequency Scaling.
AGPC	Adaptive Gain-Pulse Control.
ASM	Asynchronous State Machine.
CMOS	Complementary Metal-Oxide-Semiconductor.
DC	Direct Current.
DFS	Dynamic Frequency Scaling.
DPWM	Digital Pulse Width Modulation.
DVS	Dynamic Voltage Scaling.
EMI	Electromagnetic Interference.
MIM	Metal-Insulator-Metal.
MOS	Metal-Oxide-Semiconductor.
NMOS	N-type Metal-Oxide-Semiconductor.
PFM	Pulse Frequency Modulation.
PLS	Post-Layout-Simulation.
PMOS	P-type Metal-Oxide-Semiconductor.
PWM	Pulse Width Modulation.
SC	Switched Capacitor.
SDM	Synchronous Drive Mode.

## Symbols:

$\Delta V_{out}$	Output voltage ripple.
$\eta$	Efficiency.
$\eta_{lin}$	Linear efficiency. Max. possible efficiency for a SC DC-DC converter.
$\eta_{par}$	Efficiency of a SC DC-DC converter including only losses in conduction and parasitics (i.e. total efficiency without switching and control losses).
$\eta_{conv}$	Total efficiency of SC DC-DC converter without losses in control circuit.
$\eta_{total}$	Total efficiency of SC DC-DC converter including losses in control circuit.
$C$	Capacitance.
$E$	Energy.
$E_{cond}$	Energy lost during conduction.

$E_{ctrl}$	Energy consumed (lost) in control circuit.
$E_{in}$	Input energy.
$E_{out}$	Output energy.
$E_{par}$	Energy lost in parasitics.
$E_{sw}$	Energy lost in switching (operating the switches in the SC converter).
$f$	Frequency.
$L$	Length of the channel of a MOS transistor.
$M$	Conversion ration of a SC DC-DC converter.
$P$	Power.
$P_{in}$	Input power.
$P_{out}$	Output power.
$P_{dynamic}$	Dynamic power consumption.
$P_{static}$	Static power consumption.
$R$	Resistance.
$V_{DD}$	Supply voltage.
$V_{in}$	Input voltage.
$V_{NL}$	Output voltage at no load.
$V_{out}$	Output voltage.
$W$	Width of the channel of a MOS transistor.

# Chapter 1

## Introduction

### 1.1 Motivation

Modern technologies have enabled engineers to integrate devices with various functionalities into silicon chips that are very compact. Nowadays these devices are part of our daily life. Among the key contributors to our luxurious life style are portable devices. They have affected our life style in many ways. With recent incorporation of portable devices in medicine, the way we think about treatment of patients has expanded. Biomedical implants have offered solutions to numerous medical problems [15].

In biomedical implants, the size of the device and the battery life-time are of great importance. Since a lot of the implants tackle chronicle or permanent health issues, the implants should be as convenient as possible for the patients to live with. That is to say, smaller and lighter implantable devices are more convenient for patients. The size of implants is reduced by integrating what can be integrated of the circuitry into a single chip. While, the prolongation of the battery life is done by minimizing the power consumption of the implant's circuits as much as possible [13, 14, 33, 34] and finding other alternative power sources [9, 12, 28, 39].

Most electronic devices nowadays are designed using the CMOS technology. The power consumption of CMOS circuits is given by [36]:

$$P = P_{static} + P_{dynamic} = \frac{V_{DD}^2}{R} + fCV_{DD}^2 \quad (1.1)$$

where  $V_{DD}$  is the power supply voltage,  $R$  is the equivalent resistance of the circuit between the power supply and ground,  $f$  is the operating frequency and  $C$  is the capacitance between the output of the circuit and ground. A very interesting fact can be seen in Eq. (1.1). The power consumption of CMOS circuits is proportional to the square of the power supply voltage. Hence, if we reduce  $V_{DD}$  by a certain amount, we reduce the power consumption of the circuit quadratically. What Eq. (1.1) does not tell us is that, reducing  $V_{DD}$  might affect other circuit performance measurements. For example in digital circuits, there is a trade-off

between speed and  $V_{DD}$ . Reducing  $V_{DD}$  slows down the circuit. The other fact that can be seen in Eq. (1.1) is that, the frequency of operation is directly proportional to the dynamic power consumption. This implies that, reducing the frequency of operation of a system also reduces its power consumption. On the other hand, lower operating frequencies leads to slower systems.

Dynamic Voltage Scaling (DVS) and Dynamic Frequency Scaling (DFS) are two techniques that exploits the previously mentioned facts [25, 31, 47]. By adaptively adjusting the power supply voltage to the conditions of operation of a system, we can minimize power consumption. This is the basis of the DVS technique. Likewise in DFS, by adaptively adjusting the operating frequency of a system, or operating completely asynchronously [24], according to the workload of the system, the power consumption is minimized. These two techniques can be very helpful with extending the battery life-time in biomedical implants.

To implement the DVS technique under battery powered devices, DC-DC converters are used [10, 19, 22, 30, 40]. These converters are able to reproduce levels of DC voltages different than the input voltage (battery voltage is this case). There are various types of DC-DC converters that can be used to address the needs of the DVS technique, but since we are also considering the size of the device, we have to try to propose and demonstrate a DC-DC converter that is suitable for integration on-chip.

There are three main families of DC-DC converters: Resonant converters, Switched Capacitor (SC) converters and linear regulators [7]. The resonant DC-DC converter uses inductors and capacitors to achieve conversion. They are proven to be top notch when it comes to the conversion efficiency. However, on-chip inductors are huge, have a low quality factor, and can cause electromagnetic interference (EMI) problems [20, 44, 46]. On the other hand, linear regulators are very easy to design and integrate, But their conversion efficiency is considerably lower than the Resonant converters, especially when the output voltage is much lower than the input voltage [6, 17]. The last family of DC-DC converters is the SC DC-DC converters. It was shown in literature that this family of converters can be implemented completely on-chip while providing good conversion efficiency levels [11, 26, 29, 40, 43]. From this discussion we conclude that the most suitable family of DC-DC converters that adheres to our initial requirements is the SC DC-DC converters.

## 1.2 Objectives and Challenges

The DC-DC converter that we are designing here should handle battery powered devices, such as implants, that use DVS and/or DFS. Keeping that in mind, we will consider the following goals:

- In order to reduce the size and weight of portable device (implants), The DC-DC converter should be completely integrated on chip.
- Devices that operate with DVS requires from the DC-DC converter the ability to provide different levels of voltages from a single voltage source (in this case the battery). In addition, the change between the different levels of output voltage should be achieved as quick as possible.
- To extend the battery life-time of the powered device, the DC-DC converter should consume the lowest power possible. That implies that, the conversion efficiency under various operating conditions must be high.
- As we will explain in the coming chapters, to maximize the efficiency of a SC DC-DC converter, the operating frequency of the converter should be adapted to the loading conditions. A frequency control module should be implemented to take care of this task.
- To provide the best conversion efficiency at different levels of output voltage, the SC DC-DC converter has to adjust its switching topology. This fact will be elaborated in later chapters.
- Finally, since the circuits in battery powered implants are of low power nature, the designed DC-DC converter must maximize the efficiency around such values of power.

The list of goals that we just established faces various challenges. To fully integrate a SC DC-DC converter we will need to use on-chip capacitors. The capacitance that the on-chip capacitors provide is not as high as the capacitance of external capacitors. This has two consequences on the performance of a SC DC-DC converter; the reduction of the maximum output power that can be supplied by the SC DC-DC converter and the increase in the output ripple. The latter can be reduced by using higher switching frequencies but that solution has side-effects on other performance measurements concerning efficiency and dynamic power loss. This reduction in the maximum output power is not a main concern since we are targeting low power applications.

Improving the response time of a SC DC-DC converter is yet another challenge. In SC DC-DC converters, the response time depends on the sizes of the capacitors and switches used as well as the frequency of operation and the output power. This means that, the

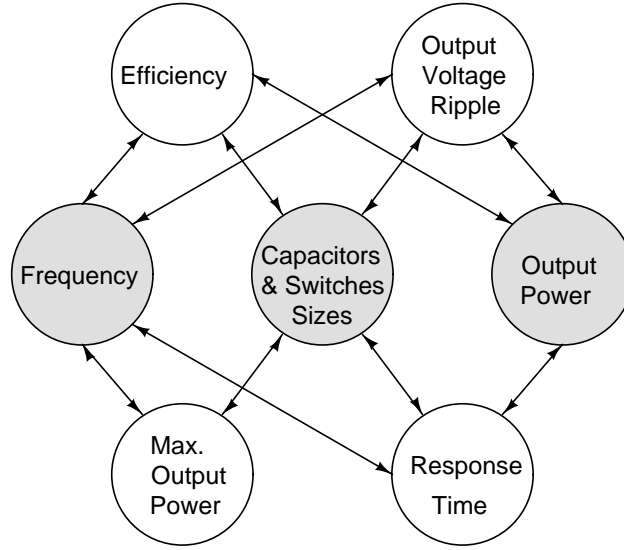


Figure 1.1 The SC DC-DC converter performance measurements and their dependence on the operating frequency, output power (output voltage and loading current) and sizes of the components

response time is also tied to a bundle of other performance measurements. In fact, all the other major performance measurements are dependent on the following parameters: the frequency of operation, output power (output voltage and loading current) and the sizes of the capacitors and switches. Note here that by "size of switches" we are referring to the width (W) and length (L) of the CMOS switches, which determines the ON resistance and the gate capacitance of the CMOS transistor.

Figure 1.1 illustrates which performance measurements depend on which parameters. This complex relationship between the performance measurements makes the design process of the SC DC-DC converter challenging. The frequency of operation and the size of components are design parameters, while the output power is a parameter that is determined solely by the load demand for power. Therefore, when trying to find an optimum, the designer have about three or more levels of sweeps. One sweep is done on the size of capacitors, and another one or two sweeps are done for determining the size of switches (NMOS, PMOS). Finally the frequency of operation is swept in a certain range to optimize the performance measurements. Furthermore, if for any reason some elements of the design changed, the optimization process might have to be redone.

The last challenge that faces this design is implementing an adaptive frequency control method. The control should consume the least amount of power while maintaining a good

level of conversion efficiency for the SC DC-DC converter. In addition, a promising strategy is to ensure that the control adapts automatically the frequency of operation to the operating conditions of the SC DC-DC converter.

### 1.3 Contributions

In light of the goals that we have set and the challenges that have been mentioned, the contributions of this thesis are as follows:

- We have designed and implemented a new fully integrated asynchronous SC DC-DC converter structure that is capable of supporting ultra-low-power systems, such as biomedical implant circuitry, with an adjustable output voltage. This converter takes advantage of variable conversion ratio and scalable operating frequency to enhance the conversion efficiency under different operating conditions. To ensure robustness of the design, the SC DC-DC converter is equipped with a synchronous back-up mode that is triggered when the loading power exceeds the maximum load current.
- Moreover, in chapter 3 and 4 we developed an asynchronous controller capable of not only automatically scaling the operating frequency but also scaling the size of the switches used depending on the loading conditions. Both of these techniques help reducing the power losses in the charge transfer switches in the converter, as well as the dynamic power losses in the controller.
- We have also constructed a smart limit detection scheme in the control to allow a Mode Detector block to identify when the loading power exceeds the maximum output power. As we will explain in the coming chapters, to control the switches' sizes, we made use of the same smart detection scheme to allow the Mode Detector to turn ON additional parallel switches when needed. We also designed the Mode Detector so that it can be very easily expanded to support as many levels of additional parallel switches as desired. This is done by simply repeating (cascading) a basic block in the Mode Detector's circuitry.

### 1.4 Thesis Organization

This master's thesis is organized as follows. First, an introduction to fundamentals of conversion mechanism and efficiency in SC DC-DC converters as well as a literature review is presented in chapter 2. Chapter 3 discusses the design of a low-power asynchronous step-down DC-DC converter for implantable devices. Chapter 4 provides additional details and results for the proposed SC DC-DC converter. A general discussion about the complete



thesis is provided in chapter 5. Finally, the thesis is concluded and future improvements are suggested in chapter 6

# Chapter 2

## Basic Switched-Capacitor Converters Principals And Literature Review

### 2.1 SC DC-DC Converters Fundamentals

A brief look on the fundamental operation of a SC DC-DC converter will help the reader to better understand the topic discussed in this thesis. Terms such as: conversion ratio, conversion efficiency and drive signals are explained in this section. Moreover, some of the recent work on step-down SC DC-DC converters are reviewed. But before proceeding, two simple questions should be answered. What is a SC DC-DC converter? And how does it convert one voltage value to another?

#### 2.1.1 Conversion Mechanism and the Conversion Ratio

A switched-capacitor (SC) DC-DC converter (may also be known as a charge pump) is a block that takes an input voltage ( $V_{in}$ ) and outputs a different value of a voltage ( $V_{out}$ ). This block consists of a network of capacitors and switches, and operates in two phases or more. If the output is higher in voltage than the input, the conversion is called a "step-up" conversion. Vice versa, if the output voltage was lower than the input, the conversion is called a "step-down" conversion. The type of conversion that we will be focusing on in this thesis is the step-down conversion.

Most of the SC DC-DC converters operate in two phases: a charging phase and a discharging phase. The charging phase takes place when a group of capacitors in the network are connected to the DC power source (input) to get charged, while the discharging phase starts when this group of capacitors are connected to the load (output) to discharge. Since these capacitors are responsible of transferring the charge from the input to the output, they are sometimes known as the charge-transfer capacitors [29, 45]. Likewise, some authors refers to them as the pumping capacitors because they "pump" the charge from the input to the output[11, 40].

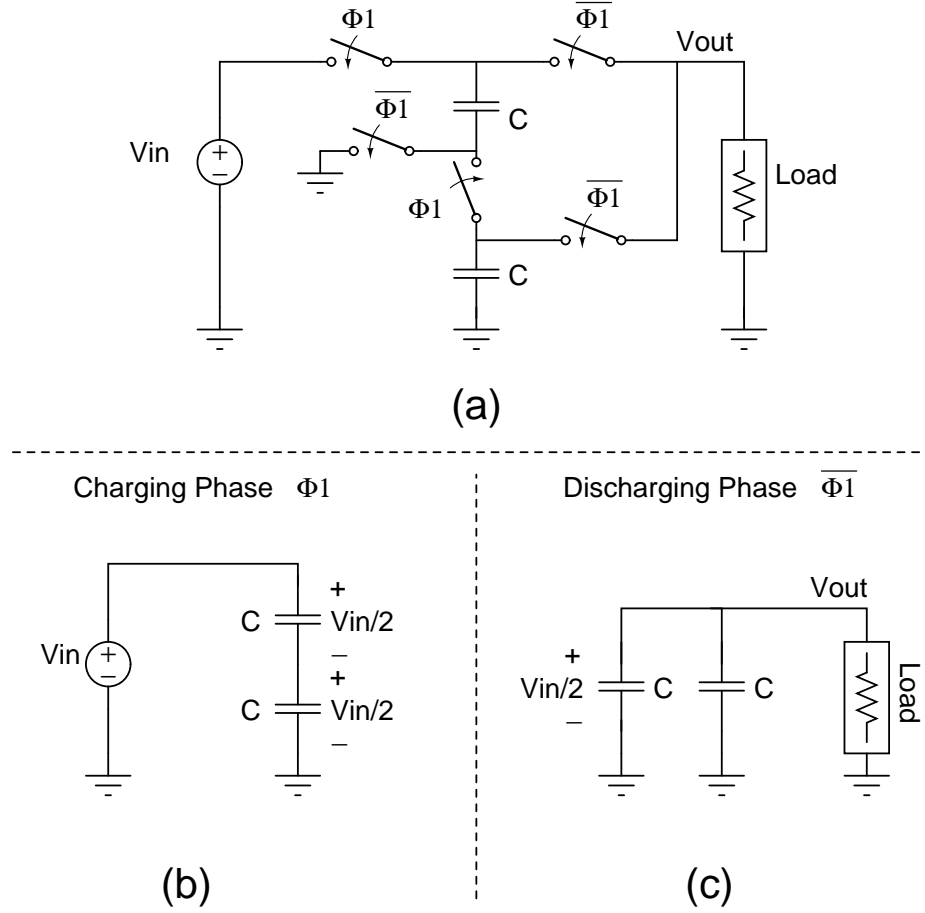


Figure 2.1 An example of the operation of a SC series-parallel configuration in stepping down an input voltage, (a) shows the complete network of capacitors and switches.  $\Phi_1$  and  $\overline{\Phi_1}$  are the control signals for the switches (b) shows the equivalent circuit when the switches controlled by  $\Phi_1$  are ON, (b) shows the equivalent circuit when the switches controlled by  $\overline{\Phi_1}$  are ON.

There may be several different configurations of connecting the capacitors in each of these phases, and each configuration has its own characteristics. In this project, we adopted the "Series-Parallel" configuration. Not only is this configuration simple, but also it offers a better performance at lower switching frequencies [37]. The reason for pursuing lower switching frequencies will be explained soon.

An example of a series-parallel step-down SC DC-DC converter is presented in Fig. 2.1. Two capacitors and five switches are connected in a network, and the switches are controlled by two signals  $\Phi_1$  and  $\overline{\Phi_1}$  (Fig. 2.1(a)). In the first phase (charging phase),  $\Phi_1$  turns ON a set of switches which will connect the two capacitors in series (Fig. 2.1(b)). Since both capacitors have the same value of capacitance  $C$ , each will be charged to  $V_{in}/2$ . Assuming of

course that enough time was provided for the capacitors to be fully charged. In the second phase, the switches connected to  $\Phi_1$  turn OFF, while the ones connected to  $\overline{\Phi_1}$  turn ON. This will connect both capacitors in parallel with the output load resulting in an output voltage  $V_{out} = V_{in}/2$ . As current starts to flow in the load, the charge stored in the capacitors will deplete and the output voltage will drop.

In the previous example,  $V_{in}$  was converted to  $V_{in}/2$ . If the load was not connected, the output voltage would have remained at half the input. The ratio of the output voltage to the input voltage, when no load is connected, is called the conversion ratio ( $M$ ).

$$M = \frac{V_{NL}}{V_{in}} \quad (2.1)$$

Notice that, the output voltage ( $V_{out}$ ) of a SC DC-DC converter with conversion ratio ( $M$ ) cannot exceed the output voltage at no load ( $V_{NL}$ ). For the last example, the conversion ratio  $M = 1/2$  and  $V_{out}$  can have a maximum value of  $V_{NL} = V_{in}/2$ . Now that we explained how the conversion is carried out in a series-parallel SC DC-DC converter, let us see what effects the efficiency in the conversion process.

### 2.1.2 Efficiency of SC DC-DC converters

In general, the conversion efficiency of any DC-DC converter can be defined as the percentage of energy delivered to the load ( $E_{out}$ ) with respect to the energy taken from the supply ( $E_{in}$ ) [30]:

$$\eta = \frac{E_{out}}{E_{in}} \times 100\% \quad (2.2)$$

where,

$$E_{out} = \int_T P_{out} dt \quad (2.3)$$

$$E_{in} = \int_T P_{in} dt \quad (2.4)$$

From this definition, if we try to derive the efficiency of the circuit in Fig. 2.1, we will find that:

$$\eta_{lin} = \frac{1}{M} \frac{V_{out}}{V_{in}} \times 100\% \quad (2.5)$$

An interesting fact can be seen in Eq. (2.5). The conversion efficiency does not depend on the size of the capacitors nor on the resistance in the charging path. Rather, the efficiency of a SC DC-DC converter only depends on  $V_{out}$ ,  $V_{in}$  and the conversion ratio  $M$ . This equation is commonly known as the linear efficiency ( $\eta_{lin}$ ). It is considered as the maximum efficiency

that a SC DC-DC converter can achieve [21, 29]. The name "linear efficiency" is given to this term because the efficiency drops linearly as  $V_{out}$  decreases. A detailed derivation of Eq. (2.5) is provided in Appendix A. To maximize the efficiency under different output voltages, the conversion ratio  $M$  should be adjusted accordingly. Moreover, by substituting Eq. (2.1) in Eq. (2.5), the linear efficiency would be written as:

$$\eta_{lin} = \frac{V_{out}}{V_{NL}} \times 100\% \quad (2.6)$$

This equation implies that the efficiency of a SC DC-DC converter is maximum when  $V_{out} = V_{NL}$ . Note that Eq. (2.5) represents the efficiency of transferring the charge (conduction) between the input and output in a SC DC-DC converter. In Eq. (2.2), If  $E_{in}$  was redefined as the sum of the energy delivered to the load ( $E_{out}$ ) and the energy wasted in the conversion process ( $E_{loss}$ ), the efficiency in Eq. (2.2) can be rewritten as:

$$\eta = \frac{E_{out}}{E_{out} + E_{loss}} \times 100\% \quad (2.7)$$

$E_{loss}$  is a combination of various kinds of loss mechanisms in a SC DC-DC converter. To enhance the efficiency of the converter, we should define these losses. in [30], Ramadass et Chandrakasan identified four different types of losses.

**Conduction losses ( $E_{cond}$ ):** The first type of losses,  $E_{cond}$ , is due to the power dissipated in internal voltage drops in the SC network. This term is the intrinsic loss that occurs when a capacitor charges from a battery (refer to Appendix A). It is the same loss that led to the definition of the linear efficiency in Eq. (2.5). It depends mainly on value of  $V_{out}$ ,  $V_{in}$  and the conversion ratio  $M$ . As discussed earlier, this loss is reduced by keeping  $V_{out}$  close to  $V_{NL}$  and using a SC DC-DC converter with variable conversion ratio.

**Parasitic losses( $E_{par}$ ):** The second term  $E_{par}$ , is the energy loss due to stray parasitic capacitances in the circuitry. Some parasitic capacitances for example, would store certain amount of energy from the source during the charging phase then discharge to ground during the discharge phase. The nature of this loss makes it very hard to control. It can depend on the technology, type of capacitors used and the configuration of the SC network. In addition, we can include current leakages in ESD protections circuitry (if any).

**Switching losses( $E_{sw}$ ):** The third loss term  $E_{sw}$ , is the energy used to operate the switches in the network. Since the switches used normally in a SC DC-DC converter are MOS switches, a certain amount voltage should be applied to the gates to turn them ON in one phase, and

then the gates are discharged to ground in the next phase. This is very similar to way the stray parasitic capacitance losses happen. One method to reduce these losses is by using smaller switches. This however increases the ON resistance of the switches, which can affect other performance measurements such as the maximum output voltage or current. A more reasonable approach is to vary the switches' size according to the load current. Another method of reducing this term is by reducing the switching frequency. Of course, since the frequency also affects other performance measurements, it suggests that potential benefits could be derived from a design based on a variable frequency approach.

**Control losses ( $E_{ctrl}$ ):** Finally,  $E_{ctrl}$  is the energy lost in the control circuitry. This term is the main reason why most new converters operate with digital control circuitry, which can be designed to have negligible static power consumption. The dynamic power consumption however is still an issue. Because all the current digital control circuits depend on a constant frequency clock, a certain amount of constant dynamic power loss exists. Traditionally, SC DC-DC converters were designed as open-loop converters where a control circuit was not needed. These kinds of losses may not be present in open-loop designs.

By combining all the losses that were mentioned above, the total conversion efficiency of the SC DC-DC converter becomes:

$$\eta_{total} = \frac{E_{out}}{E_{out} + E_{cond} + E_{par} + E_{sw} + E_{ctrl}} \times 100\% \quad (2.8)$$

Note that in Eq. (2.8), if  $E_{out}$  decreases while the energy losses are constant, the efficiency decreases rapidly. To maintain the efficiency high, the losses should also decrease as  $E_{out}$  decreases. In other words, the energy losses should scale with the output current (load). In this work we will design various techniques, such as complete asynchronous control and automatic switch size scaling, to make sure the energy losses scale with the output load. Unfortunately, the energy losses cannot be reduced indefinitely because there are some leakages and static power losses in CMOS circuits that are not avoidable.

Finally, we should mention here that the efficiency can be similarly defined using the average power instead of the energy. Both definitions will lead to the same result, but to be consistent with the analysis of the losses found in literature and the derivation of the linear efficiency presented in appendix A, the definition of the energy efficiency will be used throughout this thesis.

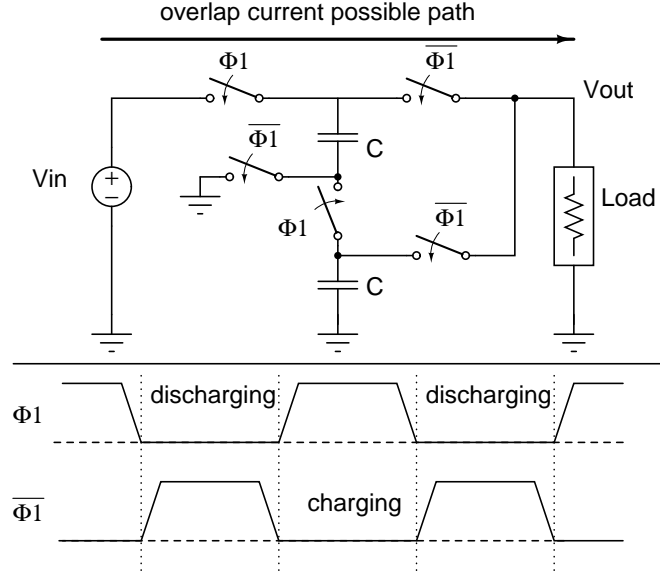


Figure 2.2 An example of a non-overlapping drive signals that should be used to avoid overlapping drive signal currents.

### 2.1.3 Drive Signal Requirements

A drive signal is the signal that controls the MOS switches in the SC DC-DC converter. Alternating between  $0V$  and  $V_{dd}$ , these signals turn ON and OFF the switches to change the connection of the capacitors in the charging and discharging phases. Typically, SC DC-DC converters operate with a drive signal and its complement. The most important requirement of these signals is to be non-overlapping. Fig. 2.2 shows an example of a SC DC-DC converter and the pattern of a drive signal ( $\Phi_1$ ) and its complement ( $\overline{\Phi_1}$ ) that should be used to drive it. If the drive signals overlap, currents may flow through undesired paths. The example in Fig. 2.2 shows one of the possible undesired paths of current that could happen if  $\Phi_1$  and  $\overline{\Phi_1}$  overlap. This path creates a connection between  $V_{in}$  and  $V_{out}$  leading to a current flowing directly from the input to the output, which reduces the conversion efficiency significantly and affects the output voltage regulation.

## 2.2 SC DC-DC Converters Control Methods

There are various control methods that exist in the literature for SC DC-DC converters. The main purpose of a control method is to regulate the output voltage at a desired level under different loading conditions. In this section, we will take a brief look at the main control methods for SC DC-DC converters, which are pulse width modulation (PWM) control and

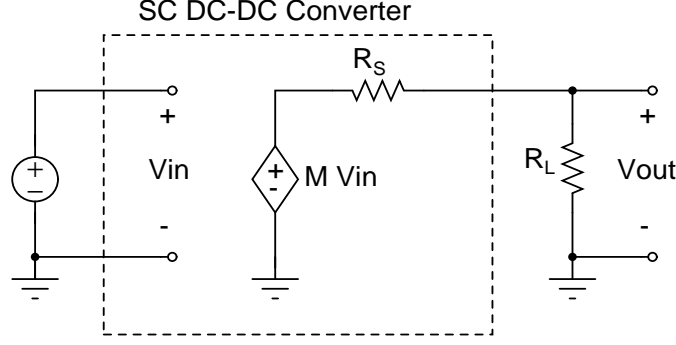


Figure 2.3 A simplified model of a SC DC-DC converter consisting of a dependent voltage source and a series resistance.

pulse frequency modulation (PFM) control. Before we go into these closed loop control methods, we will look at how an open loop SC DC-DC regulates the output voltage.

### 2.2.1 Open Loop Control

When operating a SC DC-DC converter in an open loop, the output voltage will depend on the operating frequency ( $f$ ) and the load value. To elaborate, we construct a simple model of a SC DC-DC converter consisting of a dependent voltage source with a value of  $M V_{in}$  in series with a resistance  $R_S$  (Fig. 2.3).  $M$  in this model is the conversion ratio of the converter. In Fig. 2.3, the SC DC-DC converter is loaded with a load resistance  $R_L$ . Since  $R_S$  and  $R_L$  are connected in series, they form a voltage divider. Thus, the output voltage  $V_{out}$  depends on the values of  $R_S$  and  $R_L$ . For  $V_{out}$  to be equal to  $M V_{in}$ ,  $R_L$  should have a very high impedance (No load) or  $R_S$  has to equal zero Ohms. We will see in the coming discussion that the latter is impossible. As  $R_L$  decreases (the load increases) or as  $R_S$  increases,  $V_{out}$  start to decrease below  $M V_{in}$ .

The operating frequency ( $f$ ) indirectly impacts  $V_{out}$  by affecting  $R_S$ . In 2008, Seeman and Sanders presented a detailed analysis of SC DC-DC converters [37]. One of the conclusions of their work was the fact that in a SC DC-DC converter,  $R_S$  decreases as the operating frequency ( $f$ ) increases. Once the operating frequency reaches a certain value ( $f_c$ ),  $R_S$  becomes constant (independent of  $f$ ). The value of  $f_c$  depends on the sizes of the capacitors and switches used, as well as the topology of the SC DC-DC converter. At that frequency the series resistance of the SC DC-DC converter is minimum ( $R_S = R_{SC,min}$ ). Note that for  $f < f_c$ , the output voltage ( $V_{out}$ ) is proportional to the operating frequency. This fact can be exploited to design closed loop control methods for regulating the output voltage in SC DC-DC converters.



### 2.2.2 Pulse Width Modulation (PWM) Control

One of the main control methods for regulation the output voltage in SC DC-DC converters is the Pulse Width Modulation (PWM) Control. Rather than varying the drive signal frequency to adjust the output voltage, the PWM uses a constant frequency drive signal with a variable duty-cycle. The fundamental idea of PWM is to adjust the ratio between the charging and discharging cycles, and thereby the amount of charge transferred from input to output is controlled and the output voltage is regulated at a desired level.

Unlike inductor based converters, the change in the output voltage that can be obtained from only controlling the duty-cycle in a SC DC-DC converter is limited. Hence, when the load becomes high, it is necessary to increase the operating frequency to maintain the output voltage at a constant level. This is the main disadvantage of using PWM control for this type of converters. Furthermore, this control method requires more complicated circuits and techniques than the PFM control method.

### 2.2.3 Pulse Frequency Modulation (PFM) Control

The Pulse Frequency Modulation (PFM) control method is a simple and effective way to regulate the output voltage in SC DC-DC converters. The main idea of this control method is to activate a driving signal (clock signal) when the output voltage is lower than the desired level (a reference voltage) and then deactivate it when the voltage is higher.

A basic PFM control is constructed with three basic circuits: a clock generator, a logic gate and a hysteresis comparator. The comparison between the output voltage and the reference voltage is done by the hysteresis comparator. With the help of the logic gate, the output signal from the comparator works as a mask for the clock signal allowing it to pass to the converter when the output voltage is lower than the reference, and stopping it when the output voltage is higher than the reference. Because this method of control requires a hysteresis comparator to operate, some authors call it hysteresis control [38].

One advantage of the PFM is that it can reduce the switching losses of the converter at light loads. However, the clock is constantly running, which leads to a constant dynamic power loss in the control circuit. Also, the frequency of the clock used is the maximum frequency that the PFM control can achieve. Hence, this frequency should be carefully chosen according the maximum load of the converter.

## 2.3 Literature Review

SC DC-DC converters have been around for decades. During that time, various designs were presented for various applications. Recently, researchers began to investigate the potential of integrating SC DC-DC converters both fully and partially [5, 11, 29, 40, 43, 45]. The following is a review on the main works done recently on SC DC-DC converters.

In 2005, Bin *et al.* presented a high efficiency inductorless step-down DC/DC converter. This converter is a SC DC-DC converter with variable conversion ratio (Authors call it fractional conversion ratio) [5]. It is designed to provide three different conversion ratios: 1,  $\frac{1}{2}$  and  $\frac{2}{3}$ . This converter is controlled with two feedback loops, one is a pulse-frequency-modulation (PFM) control with a base clock frequency of  $2MHz$ , and the other is a current control loop. The PFM control regulates the output voltage at light loads with constant pulse-width drive signals generated only when needed. This is used to increase the efficiency at light loads. At higher loads, the current control loop reduces the output ripple by selecting the appropriate drive signal frequency and duty cycle for each conversion ratio. External capacitances are used in this converter, while the rest of the circuitry was designed in TSMC  $0.25\mu m$   $2.5V/5V$  mixed signal CMOS process. The input battery voltage can be varied from  $2.8V$  to  $5V$  for an output of  $1.8V$ , while the maximum load current for this converter is  $100mA$  and the conversion efficiency is in the range from 85% to 65%. The controller power consumption was not included in the efficiency results. Finally, the output ripple was measured to be less than  $10mV$ .

Two years later, in 2007, Viraj and Amaratunga introduced a monolithic CMOS  $5V/1V$  switched capacitor DC-DC step-down converter [43]. Using three integrated  $400pF$  capacitors, this design was able to step-down the input voltage from  $5V$  to  $1V$ . A pulse-width-modulation (PWM) control scheme with  $25MHz$  switching frequency was adopted to regulate the output voltage. The PWM scheme regulates the output voltage by controlling the charging time of the capacitors. The whole converter was integrated with CMOS  $0.35\mu m$  P-well process with a total area of  $2.6 \times 2.6mm^2$ . It achieves a 62% efficiency when the switching losses are included, while the theoretical maximum efficiency was 80%. The tested converter runs on  $15MHz$ , instead of  $25MHz$ , due to process variation after fabrication. Neither the maximum load power nor maximum load current were provided.

Ramadass and Chandrakasan, in 2007 presented a voltage scalable switched capacitor DC-DC converter for ultra-low-power on-chip applications [29]. This design is a fully integrated SC DC-DC converter targeting systems that can apply the DVS technique to reduce power

consumption. This work describes a SC network, consisting of four capacitors, that can achieve five different conversion ratios ( $1$ ,  $\frac{3}{4}$ ,  $\frac{1}{2}$ ,  $\frac{2}{3}$  and  $\frac{1}{3}$ ). With the use of PFM control and an automatic frequency scaling (AFS) block, this converter achieved conversion efficiency in the range of  $80 - 50\%$  for load powers in the range of  $5\mu W$  to  $1\mu W$ . The AFS block can select one out of three possible switching frequencies ( $15/7.5/3.75MHz$ ), which are produced by dividing the frequency of a  $15MHz$  clock. This is done to reduce the dynamic power consumption in the control circuit at light loads. Two different levels of input voltages are required,  $1.8V$  and  $1.2V$ . The  $1.8V$  is used to drive some of the switches in the SC network, while the  $1.2V$  acts as the input voltage and supplies power for the rest of the circuitry. With these input voltages, the converter can regulate output voltages between  $1.1V$  to  $0.3V$ . The fabrication of this design was done in CMOS  $0.18\mu m$  technology and occupied a chip area of  $1.6 \times 1.6mm^2$ .

In 2008, an integrated reconfigurable switched-capacitor DC-DC converter with a dual-loop adaptive gain-pulse control was described by Chowdhury and Ma [11]. This design is built on two time-interleaved SC DC-DC converter to produce lower output voltage ripple and faster load transient. To control the converter, the authors used an adaptive gain-pulse control (AGPC). The name comes from the fact that this controller is able to automatically adjust both the pulse frequency and conversion ratio according to operation conditions. The configuration of this converter allows it to choose between conversion ratios of  $1$ ,  $\frac{1}{2}$ ,  $\frac{2}{3}$  and  $\frac{1}{3}$ . Designed in TSMC  $0.35\mu m$  CMOS N-Well Process, the converter takes input voltages in the range of  $2.1V$  to  $3.3V$  and output voltages in the range of  $0.9V$  to  $1.8V$ , with a maximum efficiency of  $76\%$  at  $39mW$  load power. The simulation under Hspice showed that this converter has a rise time of  $6.2\mu s$  when charging the output voltage from  $0.9V$  to  $1.8V$ , while the fall time happens in  $20.9\mu s$ . No information was provided about the loading conditions under which the transient test was done. However, four pumping capacitors, each with a value of  $1.5nF$ , were used with a  $10MHz$  base clock frequency.

Wenhan *et al.* presented, in 2009, a variable step-down conversion ratio switched capacitor DC-DC converter for energy harvesting systems working in intermittent mode [45]. The authors here design another SC DC-DC converter with adjustable conversion ratio with a PFM control scheme. The converter chooses one of three conversion ratios to work with ( $1$ ,  $\frac{1}{2}$  and  $\frac{2}{3}$ ). With a PFM controller operating with a base frequency of  $1MHz$ , the converter steps down input voltages in the range of  $5 - 15V$  to an output voltage of  $2V$ . The converter circuitry have been fabricated in the  $0.35\mu m$  CMOS process with EEPROM technology. The size of the core circuit is  $600 \times 800\mu m^2$ . Information about the sizes of the capacitors used

were not provided. The whole design is reported to have an efficiency in the range of 28% to 42%.

More recently, Su *et al.* published in 2010 a monolithic step-down SC power converter with sub-threshold digital-pulse-width-modulation (DPWM) control for self-powered wireless sensors [40]. A sophisticated control scheme is adopted here. The controller consists of an error processor, a proportional controller, and a DPWM modulator. To operate the DPWM, a  $200kHz$  base clock is generated with sub-threshold ring oscillators and frequency dividers. This converter was fabricated with a  $0.35\mu m$  digital n-well CMOS process. It occupies an area of  $7.8mm^2$  with two on-chip capacitors each with a value of  $3.36nF$ . The input voltage of the converter is  $2.5V$  while the output voltage can be regulated at any level between  $0.8V$  and  $1.5V$ , with a load current ranging from  $500\mu A$  to  $5mA$ . The controller is programmed to produce switching frequencies from  $200kHz$  to  $1MHz$  depending on the instantaneous loading conditions. The maximum efficiency that can be achieve in this design is 66.7% with the controller dissipating  $147.5\mu W$  of power.

All the designs discussed above presented interesting approaches for designing SC DC-DC converters, each with respective advantages and disadvantages. In [5], the authors used a current control loop with PFM which reduced the output ripple to less than  $10mV$  and resulted in a maximum efficiency of 85%. The results, however, are only based on simulations and the capacitors are not integrated on chip. On the other hand, the converter presented in [43] used a PWM control scheme and achieved a 65% efficiency experimentally with on-chip capacitors. The disadvantage of this converter is that it is designed for a fixed value of input and output voltages. By contrast, the converter introduced by [29] has a flexible range of output voltage ( $0.3V$  to  $1.1V$ ) and uses five conversion ratios to achieve good efficiency over that range of output voltage. The PFM with AFS control helped this converter achieve high efficiencies at a low load power range. This converter, however, requires two input power supplies ( $1.8V$  and  $1.2V$ ) which is not convenient for applications in electronic biomedical implants because it results in an increase in the implant size.

The AGPC presented in [11] has a unique approach for automatically adapting the pulse-frequency of the drive signal and the conversion ratio of the converter according to the load. This control method shows a good voltage tracking performance which is suitable for use in DVS. Unfortunately, only simulation results are available and the capacitors used are not designed to be integrated. Contrastingly in [45], a converter that can step-down an input voltage of  $15V$  to  $2V$  is implemented. The main advantage of this converter is that it can

operate on a very wide range of input voltages (15 to 5) using three different conversion ratios. The disadvantage is that the efficiency is not very high due to the huge gap between the input and output voltage. Finally in [40], the authors presented sub-threshold DPWM controlled SC DC-DC converter that achieves a maximum of 66.7% efficiency over a wide range of load power (0.4mW to 7.5mW) with on-chip capacitors. The disadvantage of this converter is that it uses a very complicated control method with a large number of control signals. Moreover, the efficiency is maximum around 1.3V and starts to decrease as the output voltage increases.

Table 2.1 Comparison of recent literature on step-down SC DC-DC converters

<i>Design</i>	<b>Bin 2005</b>	<b>Viraj 2007</b>	<b>Ramadass 2007</b>
<i>Technology (<math>\mu m</math>)</i>	0.25	0.35	0.18
<i>Chip Area (<math>mm^2</math>)</i>	N/A	$2.6 \times 2.6$	$1.6 \times 1.6$
<i>Active Area (<math>mm^2</math>)</i>	N/A	N/A	0.57
<i>Total On-Chip Cap (nF)</i>	N/A	1.2	2.4
<i>Num. of conversion ratios</i>	3	1	5
<i>V<sub>out</sub> (V)</i>	1.8	1	0.3 – 1.1
<i>V<sub>in</sub> (V)</i>	2.8 – 5	5	1.8 and 1.2
<i>Load power range</i>	180mW	N/A	$5\mu - 1mW$
<i>Max. output load (mA)</i>	100	N/A	0.9
<i>Efficiency range</i>	65 – 85%	62%	50 – 80%
<i>Control type</i>	PFM+Current Control	PWM	PFM+AFS
<i>Operating frequency (MHz)</i>	2	15	15/7.5/3.75
<i>On-Chip capacitors</i>	No	Yes	Yes
<i>Type of results</i>	Simulation	Experimental	Experimental
<i>Design (Continued)</i>	<b>Chowdhury 2008</b>	<b>Wenhan 2009</b>	<b>Su 2010</b>
<i>Technology (<math>\mu m</math>)</i>	0.35	0.35	0.35
<i>Chip Area (<math>mm^2</math>)</i>	N/A	N/A	7.8
<i>Active Area (<math>mm^2</math>)</i>	N/A	0.48	4
<i>Total On-Chip Cap (nF)</i>	6	N/A	6.72
<i>Num. of conversion ratios</i>	4	3	1
<i>V<sub>out</sub> (V)</i>	0.9 – 1.8	2	0.8 – 1.5
<i>V<sub>in</sub> (V)</i>	2.1 – 3.3	5 – 15	2.5
<i>Load power range</i>	N/A	$\geq 1mW$	0.4 – 7.5mW
<i>Max. output load (mA)</i>	N/A	N/A	5
<i>Efficiency range</i>	$\leq 76\%$	28 – 42%	$\leq 66.7\%$
<i>Control type</i>	Adaptive-Gain-Pulse	PFM	DPWM
<i>Operating frequency (MHz)</i>	10	1	0.2 – 1
<i>On-Chip capacitors</i>	No	N/A	Yes
<i>Type of results</i>	Simulation	Experimental	Experimental

Table 2.1 compares and summarizes the information collected in this review. From this review we concluded that, a mechanism to change the switching frequency according to the loading condition is preferable, because it mitigates switching losses in the converter. All the techniques reported use a base clock frequency to generate the different switching frequencies. The maximum output load depends on the size of the capacitors used. Furthermore, SC DC-DC converters with adjustable conversion ratios have a more dynamic range of input and output voltages. Finally, both simulation and experimental results have shown that SC DC-DC converters are suitable for implementing on-chip high-efficiency power converters.

## 2.4 Asynchronous Sequential Logic

Before proceeding with the design of the proposed SC DC-DC converter, we will introduce asynchronous sequential circuits which are at the core of the control method discussed in chapter 3. The advantages and drawbacks of asynchronous sequential circuits in relation to their synchronous counterparts are presented here, as well as the procedure of synthesizing an asynchronous state machine (ASM).

### 2.4.1 An Overview

In sequential circuits, output signals are functions of the change in input signals. To track the change in an input signal, sequential circuits include a mechanism to store the previous state of either the input signals or a function based on the input signals. The output of these functions are known as internal signals (internal states). Synchronous sequential circuits use flip-flops and a clock to store the previous state of inputs and to update outputs. Contrastingly, asynchronous sequential circuits utilize the built-in delay in logic gates to achieve the same task. This dependence on the built-in delay in logic gates makes the design of asynchronous sequential circuits more complicated than their synchronous counterpart. Also, it can cause the output to oscillate if not designed properly. On the other hand, asynchronous sequential circuits are considered faster because they do not wait for a clock pulse to update the output. This asynchronous behavior also leads to a lower dynamic power consumption. Moreover, an asynchronous sequential circuit tend to use less area to implement than synchronous ones. That is because the main building block of synchronous sequential circuits (flip-flop) is based on a simpler asynchronous sequential circuit (the SR latch).

Fig. 2.4 shows an example of an asynchronous sequential circuit. In general, any asynchronous sequential circuit consists of inputs, next state forming logic, internal states that

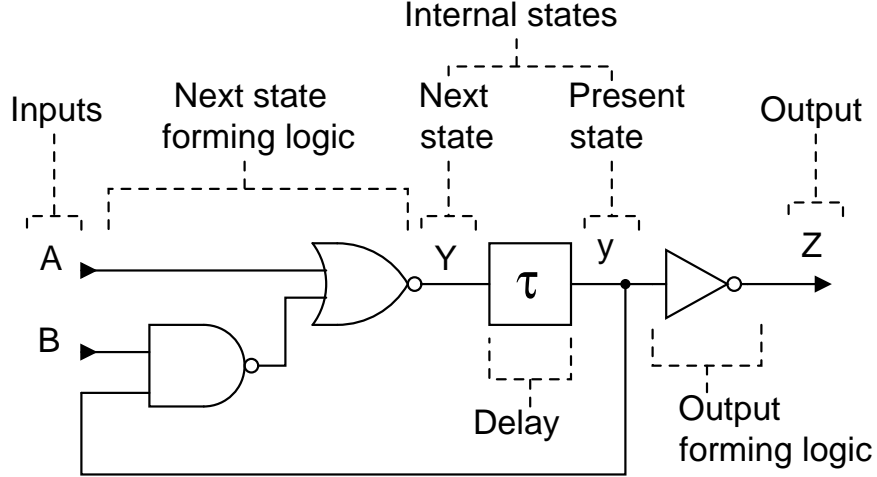


Figure 2.4 A simple asynchronous sequential circuit.

are fed back to the input, output forming logic and outputs [41]. The feedback connecting the present state with the input is one of the distinguishing features of an asynchronous sequential circuit. In this example,  $y$  represents the present state while  $Y$  is the next state. The next state ( $Y$ ) is a function of the inputs ( $A$  and  $B$ ) and the present state ( $y$ ). The delay block  $\tau$  (shown in Fig. 2.4) represents the equivalent propagation delay of the logic gates preceding it (i.e. it is not a physical component). A change occurring in  $Y$  will propagate to  $y$  after  $\tau$  seconds. The output  $Z$  of this circuit is a function of the present state  $y$  (in this example  $Z = \bar{y}$ ).

A state of an asynchronous sequential circuit is defined as a set of values of inputs, internal states (present and next) and corresponding outputs. asynchronous sequential circuits work by jumping from one state to another according to the change in the input. That is why they are also known as asynchronous state machines (ASM). In ASM, there are two types of states: a stable state and an unstable state. A stable state is the state where the value of the inputs does not change the next state ( $Y = y$ ), while an unstable state is a state where the next state changes with the inputs ( $Y \neq y$ ). Unstable states are transitional states. Meaning, they will lead to a new state (a new value of  $y$ ). The new state can be either a stable state or an unstable state. To ensue stability and to avoid oscillation in the output, the designer should make sure that all unstable states lead to a stable state.

The synthesis of an ASM can be summarized in five steps [8, 23]:

1. A state flow diagram that describes the change in the states according to the inputs is generated.

2. From the state flow diagram, a flow table is constructed. A flow table is just another representation of the state flow diagram.
3. By assigning a unique boolean value to each of the states in the flow table, an excitation table is formed.
4. Karnaugh maps that represents the next state forming logic and the output forming logic is extracted from the excitation table.
5. Boolean equations representing the next states and the outputs are extracted from the Karnaugh maps and the equivalent logic circuits are realized.

### 2.4.2 An Example of a 2-bit Counter

To elaborate the synthesis process, we will construct a simple 2-bit counter that is level triggered by an input signal  $A$ . First we will construct a state flow graph (Fig .2.5). This graph shows the four states of the 2-bit counter with outputs  $Z_1$  and  $Z_2$ , where  $Z_1$  is the most significant bit and  $Z_2$  the least significant bit. As  $A$  changes, the counter will increment the output by 1-bit, going from '00' to '11'. The next step in the synthesis process is to construct a flow table from the state flow graph (Table 2.3). In this table, the stable states are underlined. It can be seen in this table that each unstable state will lead to a stable one, and the output will not oscillate.

The next step is to assign boolean values to the states and transform the flow table into an excitation table. To do that, we will first define the present state variables  $y_1$  and  $y_2$  and the next state variables  $Y_1$  and  $Y_2$ . Then, since we have four states, we will need 2 bits to

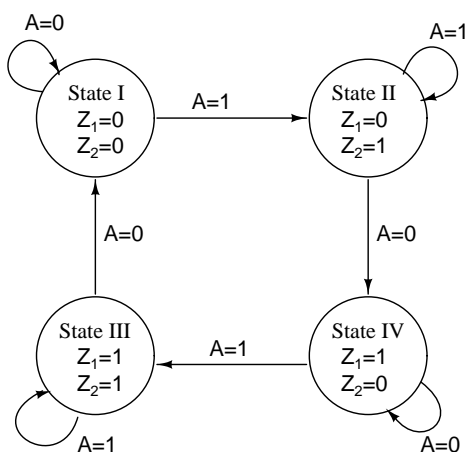


Figure 2.5 State flow graph for a 2-bit counter that is level triggered by the input signal  $A$ .



Table 2.3 2-bit counter flow table.

Present state	Next state		Output $Z_1 Z_2$
	$A = 0$	$A = 1$	
I	<u>I</u>	II	00
II	III	<u>II</u>	01
III	<u>III</u>	IV	10
IV	I	<u>IV</u>	11

Table 2.4 2-bit counter excitation table.

Present state $y_1 y_2$	Next state		Output $Z_1 Z_2$
	$A = 0$	$A = 1$	
	$Y_1 Y_2$	$Y_1 Y_2$	
00	00	01	00
01	11	01	01
11	11	10	10
10	00	10	11

represent them. We will assign the states  $I$ ,  $II$ ,  $III$  and  $IV$  to the values '00', '01', '11' and '10' respectively. When assigning values to the states, it is recommended to avoid having two consequent states that are the complement of each others. Flipping all the internal states at the same time might lead to an unexpected behavior. The excitation table of this 2-bit counter with the assigned values is shown in Table 2.4. From this table we extract Karnaugh maps for the next states  $Y_1$ ,  $Y_2$  as well as the outputs  $Z_1$  and  $Z_2$ . The result of the extraction is shown in Fig. 2.6. From these maps, the following boolean equations are found:

$$\begin{aligned}
 Z_1 &= y_1 \\
 Z_2 &= y_1 \oplus y_2 \\
 Y_1 &= A \cdot y_1 + \overline{A} \cdot y_2 \\
 Y_2 &= A \cdot \overline{y_1} + \overline{A} \cdot y_2
 \end{aligned} \tag{2.9}$$

The final step of synthesizing the asynchronous 2-bit counter is to build the equivalent digital circuit of Eq. (2.9). The circuit shown in Fig. 2.7 represent the circuit of the asynchronous 2-bit counter presented in this example.

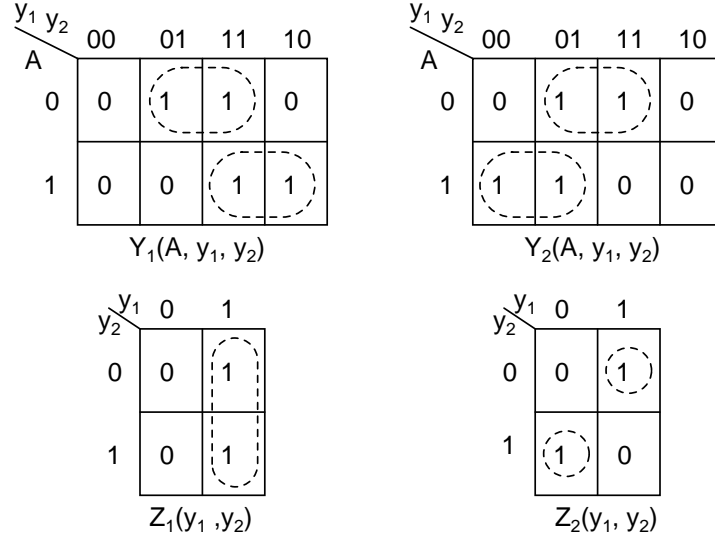


Figure 2.6 Karnaugh maps derived from the excitation table of the 2-bit counter.

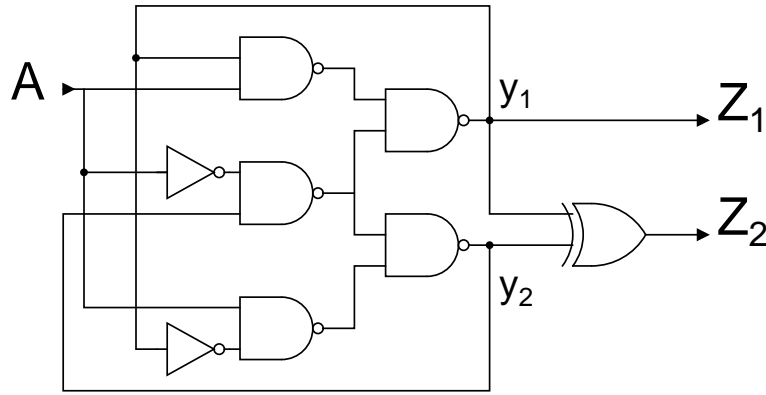


Figure 2.7 Circuit of the asynchronous 2-bit counter.

### 2.4.3 Summary

In this section, we presented an overview of asynchronous sequential circuits and demonstrated a synthesis method for ASMs. Such circuits can be challenging to design when the number of states is increased, but the benefits which they provide can be very rewarding. Asynchronous circuits are well known for their efficient use of energy [27, 42]. This is due to their event triggered operation, which does not depend on a constant running clock. As we will show in the next chapter, these type of circuits are ideal for designing a low power control method capable of generating a variable frequency drive signal for SC DC-DC converters.

# Chapter 3

## A Low-Power Asynchronous Step-Down DC-DC Converter for Implantable Devices

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### 3.1 Abstract

We present in this paper a fully integrated asynchronous step-down switched capacitor DC-DC conversion structure suitable for supporting ultra-low-power circuits commonly found in biomedical implants. The proposed converter uses a fully digital asynchronous state machine as the heart of the control circuitry to generate the drive signals. To minimize the switching losses, the asynchronous controller scales the switching frequency of the drive signals according to the loading conditions. It also turns on additional parallel switches when needed and has a backup synchronous drive mode. This circuit regulates load voltages from 300mV to 1.1V derived from a 1.2V input voltage. A total of 350pF on chip capacitance was implemented to support a maximum of 230 $\mu$ W load power, while providing efficiency up to 80%. The circuit validating the proposed concepts was fabricated in 0.13 $\mu$ m CMOS technology. Experimental test results confirm the expected functionality and performance of the proposed circuit.

**Keywords** Biomedical Devices, DC-DC power converters, Power Management, Voltage scalable switched capacitor, Dynamic voltage scaling, Asynchronous control

## 3.2 Introduction

Battery life is an important issue in all portable electronic devices. The matter becomes even more crucial when the needed portable devices are medical implants. In such devices, life itself might become dependent on the battery life. Naturally, as all battery powered devices, the battery of the implant must be replaced after a certain period of time. A frequent change of an implant's battery is not desired because it requires surgical procedure. This has driven researchers to develop powering solutions for implants [9, 28, 39]. Whether the implant is powered by a battery, inductive link, piezoelectric source or a combination of these sources, it is important to have circuits with ultra-low-power consumption that would efficiently use these energy resources. Reducing the power dissipation in these circuits also helps to reduce the risk of damaging surrounding tissues due to dissipated heat [34]. Examples of circuits that consume from several 100's of micro-watts to less than a micro-watt were developed in recent years [13, 14, 33].

One method of reducing power consumption in CMOS circuits is the Dynamic Voltage Scaling (DVS) technique [47]. This technique exploits the fact that energy consumption scales quadratically with supply voltage. Due to the trade-off between power and delay in CMOS circuits, the supply voltage is often scaled according to the needed throughput and activity. DVS can be applied by either switching between multiple DC sources [1], or by using DC-DC converters [10, 19, 26, 29, 30, 40]. The latter approach is more appropriate in the case of biomedical implants, since having more than one battery (DC source) adds to the overall weight and size of the implant. Moreover, it was shown that combining voltage scaling with self-timed systems (asynchronous) can lead to further reduction in power consumption [24].

There are various approaches to design DC-DC converters for DVS technique. The approach explored in this paper uses switched-capacitors (SC) to obtain a DC-DC converter with a variable conversion ratio. This type of converters is suitable for implants because it is efficient and can be integrated. In addition, since this type of DC-DC converter has no inductors, it is less affected by electromagnetic interference, and can be used in implants that utilize inductive links.

SC DC-DC converters usually operate on a constant frequency clock. The output power, conversion efficiency, as well as the size of the capacitors and switches selected when designing the converter, depend on the frequency of that clock. The search for the right operating frequency that maximizes efficiency with respect to the size of capacitors and switches could

be a tedious task[37]. This is also much more complex when the SC converter uses multiple topologies at different output voltages.

We propose a fully asynchronous controller that varies the frequency depending on the topology used and the output current delivered. By doing so, the controller reduces the switching to the minimum necessary, and thus, reduces the switching losses in the converter. This also means that the selection of the operating frequency here is automated. Moreover, to be able to operate over a wide range of output voltages with a good efficiency, the proposed SC DC-DC converter switches between three different topologies.

To reduce switching losses at light loads, the proposed asynchronous DC-DC converter is able to select a number of switches to operate while it keeps additional switches OFF. The converter turns ON these additional switches as the loading current increases. The proposed asynchronous DC-DC converter also invokes a method of detecting the limit of load current that can be supplied, and if needed, it can switch to a backup synchronous mode of operation.

We review in section 3.3 of this paper the fundamentals of efficiency and conversion ratio in SC DC-DC converters. An overview of the complete structure of the proposed DC-DC converter is presented in section 3.4. A detailed description of the behavior of the adopted asynchronous strategy and topology manipulation is presented in section 3.4.2. The measurement results and comparison are then provided in sections 3.5 and 3.5.2 respectively. Finally this paper concludes by summarizing the main results and contributions in section 3.6.

### 3.3 Efficiency and Conversion Ratio

In SC DC-DC converters, the efficiency depends on several factors. A fundamental factor that defines the upper limit of the SC converter efficiency is the conversion ratio  $M$ , where  $M = V_{NL}/V_{in}$  is the ratio of the output voltage at no load to the input voltage. This ratio is set by the topology of capacitors and switches used by the SC DC-DC converter. The maximum efficiency for some actual output voltage and topology is defined by [21]:

$$\eta_{lin} = \frac{1}{M} \frac{V_{out}}{V_{in}} \times 100 = \frac{V_{out}}{V_{NL}} \times 100 \quad (3.1)$$

For a given topology (a fixed value of  $M$ ), the efficiency drops linearly as  $V_{out}$  drops below  $V_{NL}$ . This is why some authors refer to this property as the linear efficiency. It is important to notice here that the maximum value for  $V_{out}$  at a given topology is  $V_{NL}$ . This leads to the conclusion that the linear efficiency is maximum when  $V_{out} = V_{NL}$ . Eq. (3.1) implies that,

in order to maximize the efficiency at different output voltages, one should construct a SC DC-DC converter with an adjustable conversion ratio.

For any DC-DC converter, the efficiency in general terms is defined as the ratio of the energy delivered to the load  $E_{out}$  to the energy taken from the source  $E_{in}$ . The input energy can also be rewritten as the energy delivered to the load plus the energy lost in the converter:

$$\eta = \frac{E_{out}}{E_{in}} \times 100 = \frac{E_{out}}{E_{out} + E_{loss}} \times 100 \quad (3.2)$$

In SC DC-DC converters, several factors contribute to the loss of energy [3, 29]. The first factor is the conduction loss  $E_{cond}$ . This loss is due to the power dissipated in internal voltage drops in the SC converter. This term depends mainly on the difference between  $V_{out}$  and  $V_{NL}$ . Theoretically, if the efficiency was calculated solely based on this loss, then it would equal the linear efficiency presented in Eq. (3.1). Thus to reduce this loss, the output voltage should be as close as possible to  $V_{NL}$ . A variable conversion ratio converter approach should be used to reduce this loss over a wide range of output voltages. The second contributor to the energy lost in SC DC-DC converters is the parasitic loss  $E_{par}$ . This is the energy lost due to charging parasitic capacitances in the SC circuitry in the charging phase, then discharging them to ground in the other phase. This loss is very hard to control and could depend on the type of capacitors used and how the capacitors are connected in the charge and discharge cycles. Authors of [29] used a special pattern of drive signal to reduce this loss. Still, this technique resulted in a gain of only 3-5% in efficiency at some output voltages.

The third loss factor is the switching loss  $E_{sw}$ . This is the energy used to operate (i.e. drive or switch ON) the switches in the network. Since this part of the input energy is not going to the output of the converter, it is considered as a loss. Although this term cannot be eliminated from the equation, some remedies exist to reduce its effect. For example, varying the switches' size depending on the load current or having a variable switching frequency can help to scale  $E_{sw}$  with respect to  $E_{out}$ . This is based on the fact that  $E_{sw} = C_g V_{dd}^2$ , where  $C_g$  is the gate capacitance of the MOS switches. Further discussion about these approaches to reduce losses will take place in the following sections. The last type of losses  $E_{ctrl}$  is related to the control circuit of the converter. This loss is the main reason why recent SC converters operate with digital control circuitry, since they can be designed to have negligible static power consumption, unlike their analog counterparts. The dynamic power consumption however is still an issue.

For the sake of analyzing the contribution of each of these source of losses on the efficiency in the proposed converter, we will define the following efficiencies:

$$\eta_{par} = \frac{E_{out}}{E_{out} + E_{cond} + E_{par}} \times 100 \quad (3.3)$$

$$\eta_{conv} = \frac{E_{out}}{E_{out} + E_{cond} + E_{par} + E_{sw}} \times 100 \quad (3.4)$$

$$\eta_{total} = \frac{E_{out}}{E_{out} + E_{cond} + E_{par} + E_{sw} + E_{ctrl}} \times 100 \quad (3.5)$$

Where  $\eta_{total}$  is the total efficiency of the converter,  $\eta_{conv}$  is the efficiency of the converter without considering the energy used by the control circuitry ( $E_{ctrl}$ ) and  $\eta_{par}$  is the efficiency of the converter without considering the losses in operating the switches ( $E_{sw}$ ) nor the loss in the control circuitry ( $E_{ctrl}$ ). When each of the efficiencies defined in Eqs. (3.3), (3.4) and (3.5) is compared with the theoretical maximum efficiency ( $\eta_{lin}$ ), a better understanding can be obtained about the dynamics of the losses in efficiency with respect to other parameters, such as the loading current and the output voltage. Also, note that to measure these efficiencies we will need to measure  $E_{sw}$  and  $E_{ctrl}$ . This is done by having separate power pins for the drivers of the switches and the control circuit. On the other hand, it is impossible to measure  $E_{cond}$  and  $E_{par}$  directly. They are always measured as in  $E_{in} = E_{out} + E_{cond} + E_{par}$ .

## 3.4 Proposed DC-DC Converter

Traditionally, a SC converter would consist of a network of capacitors and MOS switches driven by two complementary clock signals. The frequency of the two complementary clock signals along with the conversion ratio of the SC converter and the output load value will set the output voltage, conversion efficiency and output ripple.

### 3.4.1 Structure overview of the converter circuit

Unlike the simple open loop structure that is used in traditional SC DC-DC converters, the proposed structure provides a more complex closed loop approach to improve robustness, controllability and performance of the converter. Fig.3.1 provides an overview of the proposed structure. In this structure, a network of SC DC-DC converters is used. This block is responsible for stepping down the input voltage to the desired output voltage value. It can support three different conversion ratios and is driven by three signals from the feedback loop.  $T_1$  and  $T_2$  are two digital signals that determine which topology the SC DC-DC

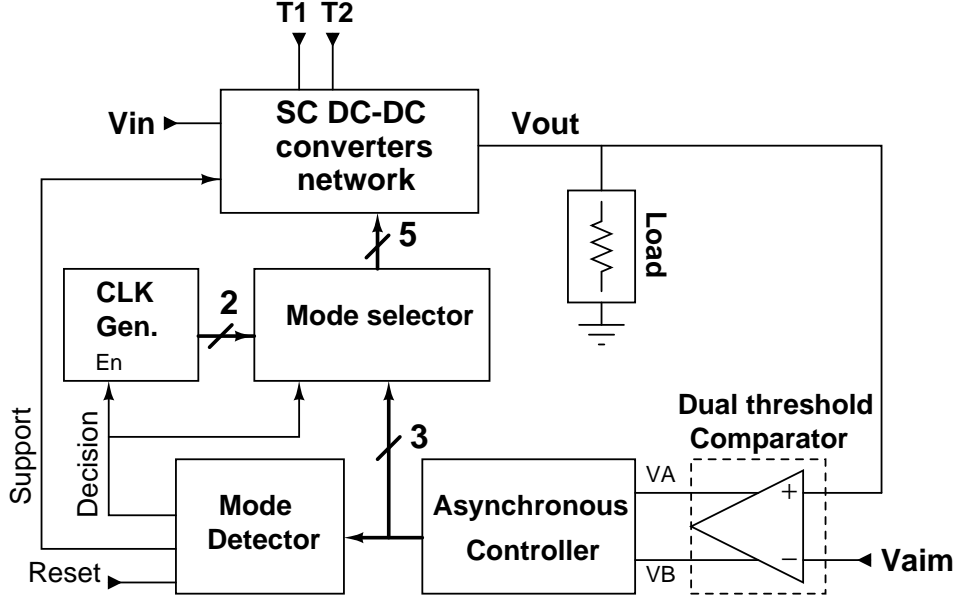


Figure 3.1 Overview of the structure of the proposed asynchronous DC-DC converter.

converter adopts to step down the input voltage. In other words, the combination of  $T_1$  and  $T_2$  selects the conversion ratio. The three possible conversion ratios are 1,  $\frac{2}{3}$  and  $\frac{1}{3}$ . The fourth combination of  $T_1$  and  $T_2$  disables the converter.

The output voltage is fed back through a comparator. Using an OTA and current mirrors, this comparator provides two output signals triggered at two different threshold voltages. Throughout this paper, we will use the word threshold voltage as a property of the comparator circuit. This should not be confused with the intrinsic threshold voltage of a MOS transistor. Moreover, this comparator should not be confused with a hysteresis comparator, and thus the following control method, although similar, is not a hysteresis control.  $V_A$  and  $V_B$  are the two digital signals that the comparator generates, while  $V_{aim}$  is the targeted output voltage of the converter.  $V_A$  is the result of the comparison between  $V_{out}$  and  $V_{aim}$ , while  $V_B$  is generated at a threshold lower than  $V_{aim}$  by almost 0.1V. The controller is an asynchronous state machine that generates the drive signals  $S_0$ ,  $S_1$  and  $S_2$  based on the signals received from the comparator. Unlike hysteresis control that results in pulses with fixed pulse-width and varying frequency, the generated drive signals are digital signals that vary in frequency and pulse width according to the variations in output load. If the load is drawing a large current, the voltage on the output capacitor will drop rapidly, making the Asynchronous Controller generate higher frequency signals. Likewise, if the load is drawing a small current, the asynchronous drive signals will have a lower frequency. Ideally, if the load draws zero



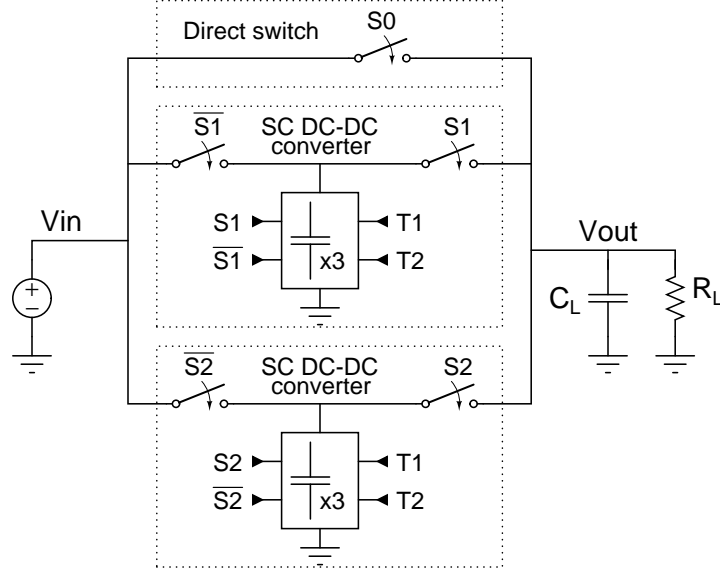


Figure 3.2 Simplified architecture of the SC DC-DC converters network.

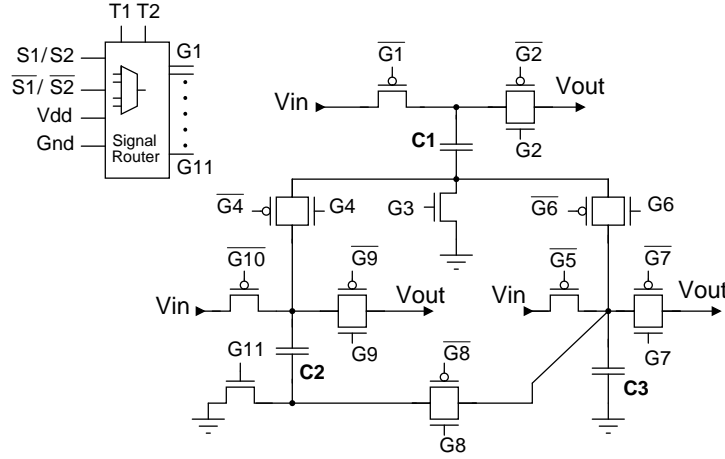


Figure 3.3 Arrangement of switches and capacitors in the SC converter.

current, no switching will happen in the drive signals. Moreover, these drive signals control the switching of the whole structure. Thus, at no load, there is no switching, so there are no switching losses or dynamic losses anywhere in the proposed structure.

The proposed structure has two modes of operation: the Asynchronous Drive Mode (ADM) and the Synchronous Drive Mode (SDM). The ADM is the main mode of operation while the SDM serves as a back-up mode. This back-up mode is triggered only if the load current goes higher than the designed limits. As we will show later on, this is done to reduce the output voltage ripple when the load draws a large current.

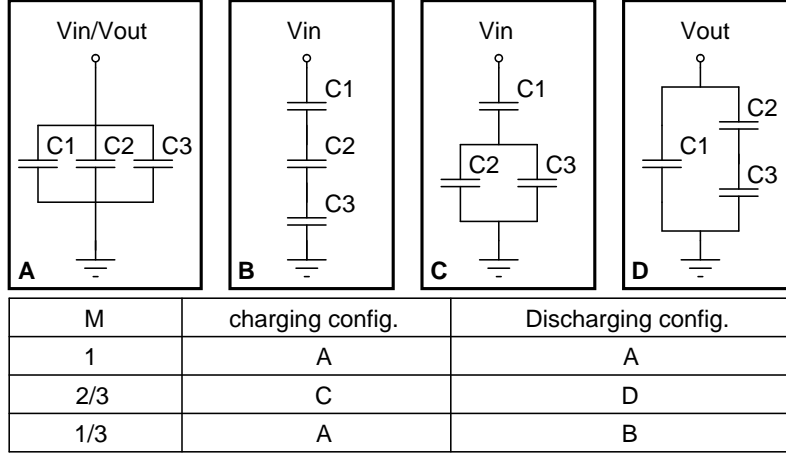


Figure 3.4 Possible topologies that can be realized with the arrangement of capacitors and switches shown in Fig. 3.3. M represents the conversion ratio achieved when switching between two of the shown arrangements.

The Mode Detector and Mode Selector are the blocks which govern the selection of the appropriate mode of operation. The Mode Detector inspects the pattern of the signals issued by the Asynchronous Controller. Depending on the size of the capacitors and switches used and the topology used to connect them, there is a limit on how much charge can be delivered to the load. When the load current exceeds the capabilities of the SC converter network, the pattern of the signals  $S_0$ ,  $S_1$  and  $S_2$  changes. These changes will be detected by the Mode Detector which will issue the *Support* signal. When the *Support* signal is high, additional switches will be turned ON in the SC converter network to decrease the output resistance. When the additional switches make the SC converter able to support the high load demands, the pattern of  $S_0$ ,  $S_1$  and  $S_2$  will go back to normal and the structure will stay in ADM. On the other hand, if the additional switches did not solve the issue, the *Decision* signal is triggered and the structure will operate under the SDM. When the structure operates with SDM, a clock generator will be enabled and the Mode Selector will forward two non-overlapping clock signals to the SC converters network. Once the load current is back to normal values, the Mode Detector can be reset and the structure will operate again with the ADM.

### 3.4.2 Asynchronous Control strategy

Before beginning to explain the details of the asynchronous control strategy that is presented here, it is essential to understand the architecture of the SC DC-DC converters network. In Fig.3.2 a simplified architecture of the SC DC-DC converters network is shown. It

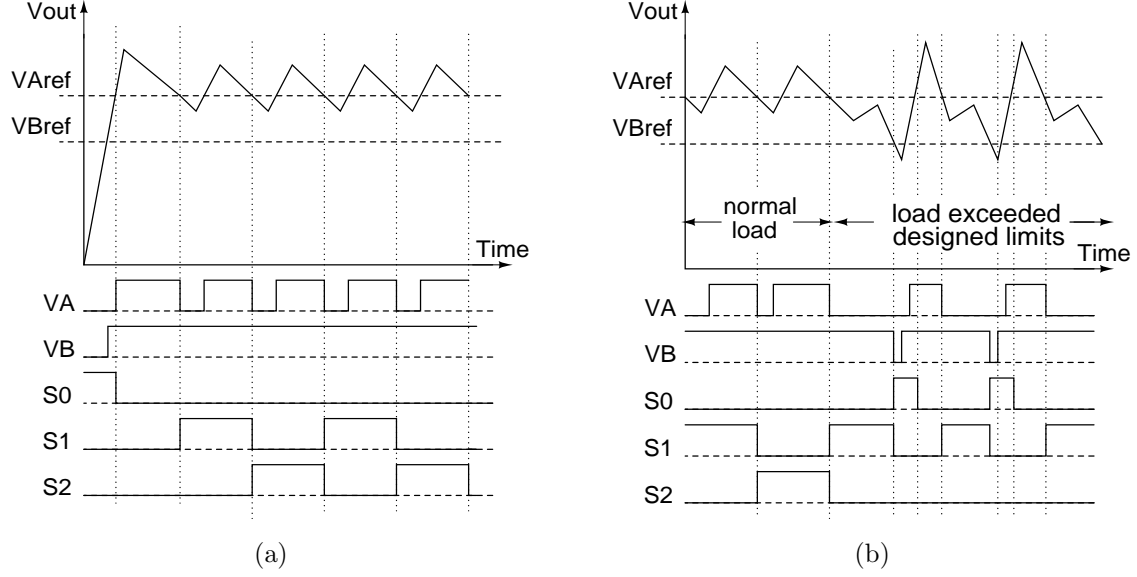


Figure 3.5 Timing diagram when the converter operates under: (a) regular load, (b) load that exceeds the limits.

can be seen that there are three ways in this network for charges to be transferred between the input and output. Either through one of the two SC DC-DC converters, or through the direct switch. The direct switch is a PMOS transistor that is used to initialize the output capacitor to the reference voltage. One of the SC DC-DC converters is driven by  $S_1$  and its complement, while the other is driven by  $S_2$  and its complement.

Each of the SC DC-DC converters is an arrangement of three capacitors connected by eleven switches (Fig.3.3). The switches are made of a PMOS transistor, a NMOS transistor, or a transmission gate depending on its location in the circuit. The switches are controlled by the signal router. Depending on the states of  $T_1$  and  $T_2$ , the signal router will provide each switch with one of its four input signals (as shown in Fig.3.3). Switches will either be ON or OFF, under the control of a drive signal or its complement, depending on the conversion ratio that is selected by  $T_1$  and  $T_2$ . To provide a conversion ratio of 1,  $\frac{2}{3}$  or  $\frac{1}{3}$ , the capacitors are connected in one of the series parallel combination that are shown in Fig 3.4.

The asynchronous control scheme depends on the signals generated by the dual threshold comparator. The two signals  $V_A$  and  $V_B$  are generated by the comparator at thresholds  $V_{Aref} = V_{aim}$  and  $V_{Bref} = V_{aim} - 0.1$ , respectively.

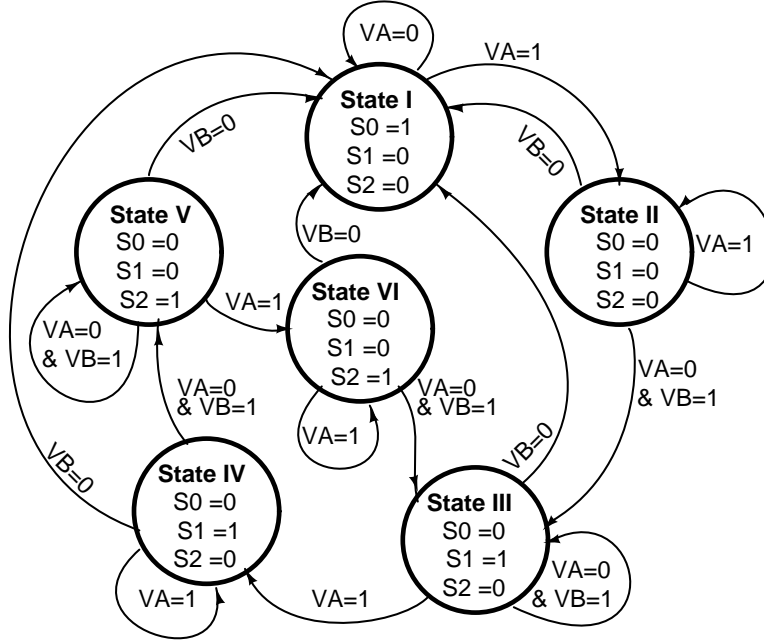


Figure 3.6 The state-flow diagram of the asynchronous controller.

Triggered by these two signals the Asynchronous Controller operates the SC converter network as follows (refer to Fig 3.5(a)). When the circuit first starts, the controller senses that  $V_{out}$  is less than both thresholds and sets the drive signals so that the output and the two SC converters starts to charge. At this stage, the output is charged directly from the input via the direct switch, which makes the charge up time very short. Once  $V_{out}$  reaches  $V_{Aref}$ , an overshoot in the output voltage will take place. During that period, the controller will turn OFF the direct switch while keeping the SC converters charging. As the load consumes the accumulated charge on the output capacitor, the output voltage will decrease until it reaches  $V_{Aref}$  again. As the output voltage starts to drop below  $V_{Aref}$ , the controller connects the first SC converters to the load. At normal loading conditions, the charge stored in SC converter will be sufficient to pull the output voltage once again above  $V_{Aref}$ . The connected SC converter will supply the output with the needed charges to sustain  $V_{out}$  above  $V_{Aref}$  until the load consumes some part of the available charge. When the output voltage drops again below  $V_{Aref}$ , the controller will switch the output to the other SC converter, while the previous converter recharges. From this point on, the controller will continue to interleave both converters to supply the load.

As the load current increases, the system will reach a point where a fully charged SC converter cannot pull up the output voltage above the threshold (refer to Fig.3.5(b)). This means that the controller cannot detect any change in the output voltage and will keep the

current SC converter connected to the load. As the charge in the SC converter depletes, the output voltage will start to decrease until it reaches  $V_{Bref}$ . This threshold serves as a safety net for  $V_{out}$ . When the output voltage goes below  $V_{Bref}$ , the controller will reset and activate the direct switch while recharging both SC converters. This will pull back  $V_{out}$  to  $V_{Aref}$  and the controller will attempt to support the load again with the SC converter.

The generation of the drive signals  $S_0$ ,  $S_1$  and  $S_2$  with respect to  $V_{out}$  and the two thresholds  $V_{Aref}$  and  $V_{Bref}$ , is shown in the timing diagram in Fig.3.5(a) and Fig.3.5(b). Also, As mentioned previously, the Asynchronous controller is a fully digital asynchronous state machine. The state-flow diagram shown in Fig.3.6 represents the behavior of the Asynchronous controller with respect to the trigger signals  $V_A$  and  $V_B$ .

### 3.4.3 Load limits detection and operation mode selection

As we have shown previously, the proposed converter has a maximum current that it can supply while regulating a certain output voltage. The maximum load current of the proposed converter can be defined as: the output current value that will prevent accumulation of enough charge on the load capacitance to allow  $V_{out}$  to cross  $V_{Aref}$ . The output voltage dynamics depends on the rate of charge and discharge occurring at the output. Thus, the maximum current that can be handled by the converter at a certain voltage depends on the topology (conversion ratio), the sizes of the capacitors and switches in the SC converter and the output capacitor size.

The block that is responsible for determining whether the SC converters are able to support the load or not is the Mode Detector. It can indirectly determine whether the load current exceeded the capabilities of the SC converter by inspecting the pattern of the drive signal generated by the Asynchronous controller. As seen previously in Fig.3.5(b), the pattern in the drive signals  $S_0$ ,  $S_1$  and  $S_2$  changes when the SC converter cannot support the load. Under normal loading conditions, the signals  $S_1$  and  $S_2$  alternate, while  $S_0$  stays low. Once the load exceed the limits, pulses in  $S_0$  will start to appear and  $S_2$  will stay low. It is important to mention that the Asynchronous controller always activates the converter driven by  $S_1$  after using the direct switch (which is driven by  $S_0$ ).

The Mode Detector shown in Fig.3.7 is built to detect that pattern. Initially when the Mode Detector is Reset, Transistors  $M_1$ ,  $M_6$ ,  $M_{10}$  and  $M_{15}$  will turn ON. This initializes all the latches in the circuit and resets the *Support* and *Decision* signals to low. As the Mode Detector is enabled, it deactivates all the reset transistors and activates  $M_2$ ,  $M_7$ ,  $M_{11}$  and

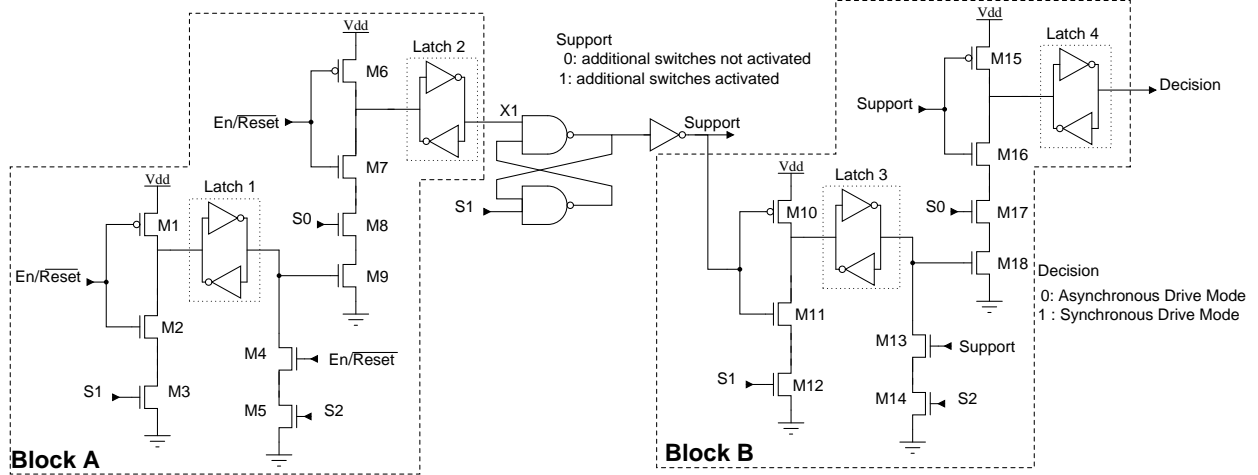


Figure 3.7 The Mode Detector circuit showing all blocks and signals used in the processes of issuing the signals *Support* and *Decision*.

$M_{16}$ . The normal pattern will start with  $S_1$  going high while  $S_0$  and  $S_2$  are low.  $S_1$  will turn ON  $M_3$ , which sinks the current in the branch and flips the state of Latch 1 to make the voltage on the gate of  $M_9$  high.

Now that  $M_9$  is ON, there are two possible scenarios. Either  $S_2$  will become high while  $S_1$  goes low, thus the loading current is within limits. Or if the load current exceeds the limits,  $S_0$  will become high and  $S_1$  goes low. In the first case,  $M_5$  will turn ON and pull down Latch 1 back to its initial state, which turns OFF  $M_9$ . As  $S_1$  and  $S_2$  alternate, Latch 1 will keep changing state and the *Support* signal will stay low. In the second case,  $M_8$  will turn ON and flip the state of Latch 2, raising the potential on node  $X1$ . If  $S_1$  overlaps with the *Support* signal when they are both high, Latch 3 in block B will flip state, leading to an error in detection. For that reason, cross coupled NAND gates are added between block A and block B to guarantee that  $S_1$  reaches a sufficiently low potential before switching *Support* to high.

When the *Support* signal is high, the SC DC-DC converter turns ON additional switches to support the required high loading current, and the second stage of the Mode Detector is activated. If this modification of the configuration was effective, the pattern in the signals will go back to normal and the *Decision* signal will stay low. On the other hand, if the load is still beyond what the SC DC-DC converters can support, the pattern will be detected by the second stage of the Mode Detector (Block B) in the same fashion. Once the *Decision* signal goes high, the converter will switch to SDM.

Notice that block A and block B in the Mode Detector are exactly the same. One of the most interesting properties of the proposed Mode Detector is that it can be expanded to support multiple stages of additional switches by simply cascading this basic block. Adding extra parallel switches reduces the output resistance of the DC-DC converters which reduces their voltage drop. This helps  $V_{out}$  to reach  $V_{Aref}$  faster. On the other hand, having more switches, leads to an increase in the switching losses, which reduces the overall efficiency. For that reason, adding switches only when needed helps keeping the overall efficiency high under light loads. Here we have demonstrated this operation in the Mode detector using one additional group of parallel switches. This can be easily expanded as we mentioned earlier, by simply cascading a number of the basic block equivalent to the number of groups of parallel switches needed, while separating the basic blocks with cross-coupled NAND gates (as demonstrated in Fig.3.7). Another issue left for further research is the exploration of strategies for rolling back the operation to the smallest feasible switch size when the load goes down for long enough. At this time, that is left to external control.

If the *Decision* signal is high, the Mode Selector will begin to drive the converter using a constant frequency clock signal. The Mode Selector consists of three multiplexer circuits combined with non-overlapping signal generators. The Mode Selector takes in the three drive signals  $S_0$ ,  $S_1$  and  $S_2$  from the Asynchronous Controller and two complementary clock signals  $CLK$  and  $\overline{CLK}$  from the clock generator. In ADM, the Mode Selector forwards the signals  $S_0$ ,  $S_1$ ,  $\overline{S_1}$ ,  $S_2$  and  $\overline{S_2}$  to the SC DC-DC converters network. Here  $\overline{S_1}$ ,  $\overline{S_2}$  are non overlapping complements of signals  $S_1$  and  $S_2$ . In SDM, the Mode Selector forwards the signals  $CLK$  and  $\overline{CLK}$  to the SC DC-DC converters network, while turning OFF the direct switch.

### 3.5 Experimental Results

The proposed converter was designed, simulated and fabricated in IBM-PDK CMOS  $0.13\mu m$  technology. The simulation and post layout results were presented in [2], and here we present our measurement results. The complete proposed structure except the clock generator have been integrated on chip (Fig.3.8). The total area of the die is  $1.5 \times 1.5 mm^2$ , whereas only  $0.52 mm^2$  was used for the active circuits and capacitors. The converter uses on chip dual MIM-capacitors (metal insulator metal capacitors) with a total value of  $350 pF$ , where each sub converter uses  $150 pF$  and the remaining  $50 pF$  is used as an output capacitor. These capacitors occupy about 10% of the total area of the die. The load current that can be supplied by this converter varies with the topology used and the output voltage value. The maximum load current that can be supplied at a nominal output voltage is  $240 \mu A$ . This can

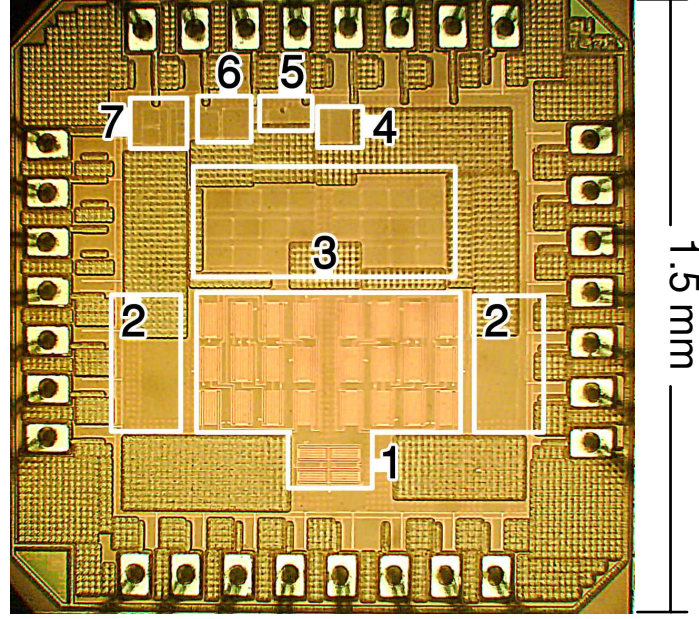


Figure 3.8 Photomicrograph of the proposed converter. The main building blocks are numbered as follows: (1) Capacitors, (2) Switches, (3) Signal router, (4) Mode detector, (5) Comparator, (6) Asynchronous controller and (7) Mode Selector

be easily increased by increasing the sizes of the capacitors used. The converter operates on a 1.2V power supply and can provide output voltages from 300mV to 1.1V. The frequency of the CLK signal in the SDM was chosen to be 4MHz. The choice was based on the frequency that created a smooth transition between the two modes of operation under the three conversion ratios. Regulation of the output in ADM at different voltages while loaded with 10K $\Omega$  and 100pF is shown in Fig.3.9. Fig.3.9(a) shows a measured settling time of approximately 408ns when going from 0V to 0.95V at start up. This fast start up response is due to the direct switch that was added in parallel to the SC DC-DC converters. The direct switch also results in faster charge up when going from low voltages to higher ones. At steady state, the controller adapts the operation frequency to the lowest frequency needed to keep  $V_{out}$  at  $V_{aim}$  under certain loading condition. Fig.3.9(b), Fig.3.9(c) and Fig.3.9(d) show the output voltage, output voltage ripple and frequency of the drive signal. The efficiency of the converter changes with the topology used, the loading current and the output voltage.

In Fig.3.10, the efficiency is plotted against the load current for six different output voltages. The efficiency graphs at  $V_{out}$  equal to 1V and 0.95V are plotted when the converter is using a conversion ratio of 1. While the efficiency graphs plotted at  $V_{out}$  equal to 0.65V and 0.6V are plotted when the converter is using a conversion ratio of  $\frac{2}{3}$ , and the remaining two graphs at  $V_{out}$  equal to 0.35V and 0.3V are plotted when the converter targets a conversion ratio of  $\frac{1}{3}$ .



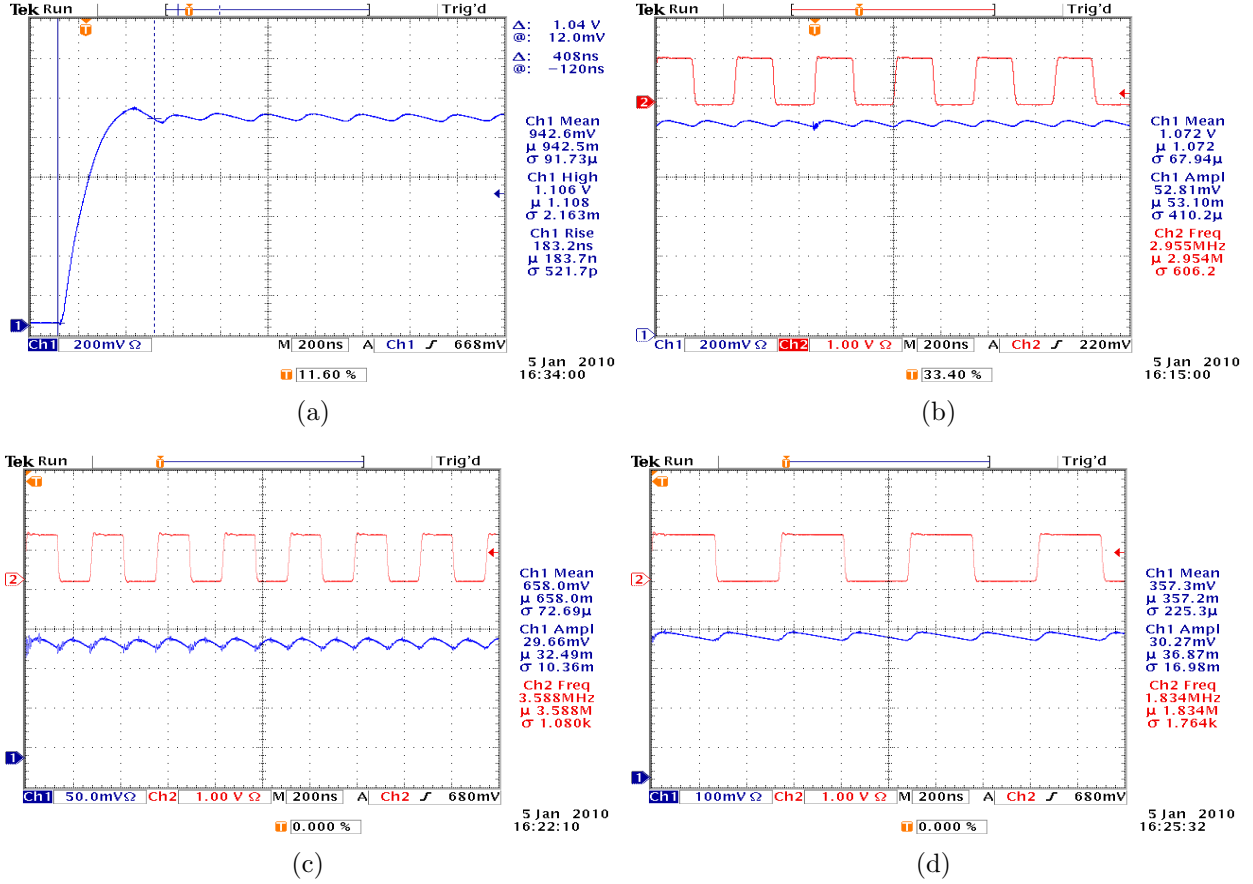


Figure 3.9 Measurement of the output voltage and the drive signal  $S_1$  of the converter while loaded with  $10k\Omega$  and  $100pF$ : (a) shows the output voltage start up response from  $0V$  to  $0.95V$  with a settling time of  $408ns$ , (b) presents the regulation at  $V_{out} = 1.07V$  with a peak to peak output ripple of  $53mV$  while the asynchronous drive signal frequency is  $3MHz$ , (c) presents the regulation at  $V_{out} = 0.66V$  with a peak to peak output ripple of  $36mV$  while the asynchronous drive signal frequency is  $3.6MHz$ , (d) presents the regulation at  $V_{out} = 0.36V$  with a peak to peak output ripple of  $32mV$  while the asynchronous drive signal frequency is  $1.9MHz$ .

The stated voltage is the control value imposed on  $V_{aim}$  in Fig.3.1. As the system is a high gain closed loop, the output voltage remains more or less independent of the load current, however, the efficiency varies. Moreover, each of the efficiency graphs shows four curves:  $\eta_{lin}$ ,  $\eta_{par}$ ,  $\eta_{conv}$  and  $\eta_{total}$  each of these efficiency terms where defined in section 3.3. This was done for several reasons. First, it allows us to see how much of the efficiency is wasted on parasitic, switching losses and control circuit. Secondly, it shows the gain in efficiency when reducing the switch sizes at lighter loads. When looking at Fig.3.10(c) and Fig.3.10(e), the reduction in  $\eta_{conv}$  from P1 to P2 or from P3 to P4 occurs when the switches sizes are increased (i.e. additional parallel switches are turned ON). Moreover, In Fig.3.10, the efficiency curves

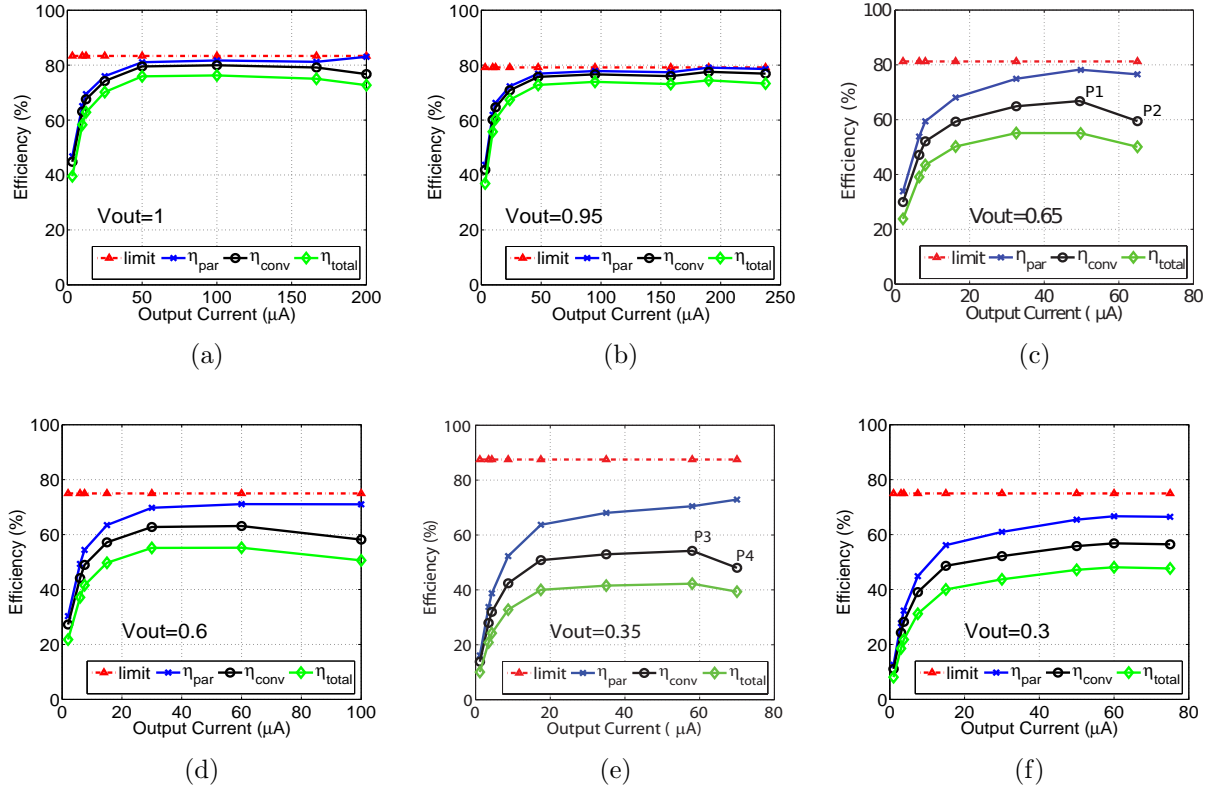


Figure 3.10 The graphs show results of the efficiency measurements versus the load current at different output voltages. The three types of efficiency defined in section 3.3 are shown in each subfigure: (a) presents the efficiencies at  $V_{\text{out}} = 1\text{V}$ , (b) presents the efficiencies at  $V_{\text{out}} = 0.95\text{V}$ , (c) presents the efficiencies at  $V_{\text{out}} = 0.65\text{V}$ , (d) presents the efficiencies at  $V_{\text{out}} = 0.6\text{V}$ , (e) presents the efficiencies at  $V_{\text{out}} = 0.35\text{V}$ , (f) presents the efficiencies at  $V_{\text{out}} = 0.3\text{V}$ .

are almost parallel, implying that the switching losses and the controller consumption scales down as the loading current scales down. This is the main advantage of driving the entire converter asynchronously. Additionally, for each conversion ratio, the switching frequency scales with the output voltage. Adapting the switching frequency to the output voltage helped maintaining the total efficiency of the converter at similar values. The effect of this operation can be seen when comparing for example Fig.3.10(e) and Fig.3.10(f). The curves of efficiency in both figures have similar values even though the theoretical maximum efficiency (limit) has dropped.

Fig.3.11 shows the measurement results of line and load regulation of the converter. The line regulation, shown in Fig. 3.11(a), is done at an output voltage of  $0.53\text{V}$  with an input step from  $1\text{V}$  to  $1.2\text{V}$  resulting in a  $16\text{mV}$  change in the output voltage. This shift in the

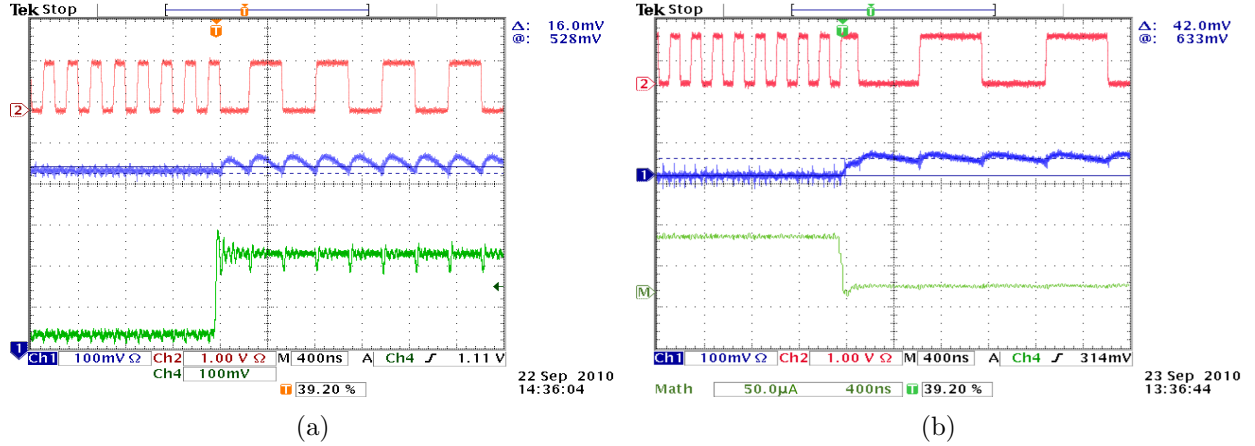


Figure 3.11 Measurement of (a) line regulation at an output voltage of  $0.53V$  with an input step from  $1V$  to  $1.2V$  resulting in a  $16mV$  change in the output voltage, (b) load regulation at an output voltage of  $0.63V$  with a load step from  $68\mu A$  to  $1\mu A$  resulting in an  $42mV$  change in the output voltage. In both measurements, the variations in the drive signal's frequency is apparent.

output voltage is due to the increase in the output ripple, which is a result of the increase charge on the charge-transfer capacitors. Fig.3.11(a) also shows a smooth transition in the output voltage and drive signal frequency during the step of the input voltage. In Fig. 3.11(b), the load regulation measurement is done at an output voltage of  $0.63V$  with a load step from  $68\mu A$  to  $1\mu A$  resulting in an  $42mV$  change in the output voltage. This figure also displays the change of the drive signal frequency when the output load changes.

More measurements on the change of the drive signal frequency with respect to the load is shown in Fig.3.12. In this Figure, the frequency is plotted versus the load at output voltages of  $0.3V$   $0.6V$  and  $0.95V$  with conversion ratios of  $\frac{1}{3}$ ,  $\frac{2}{3}$  and  $1$ , respectively. The point at which the additional switches are turned ON is indicated on the graph and it shows a slight decrease in the driving frequency due to the decrease in the equivalent resistance of the switches.

### 3.5.1 Discussion

Before we proceed any further, some points and results of the design should be discussed. In an ideal DVS situation, the voltage source is required to switch between different voltage instantaneously to provide the best energy saving. This drove us to choose a fast charge up in the converter using the direct switch. In this prototype, the direct switch was sized to be able to charge the output capacitor to the highest voltage ( $1.1V$ ) at worst case load ( $250\mu A$ ). This choice leads to bigger initial overshoot when charging at lower output voltages. A simple

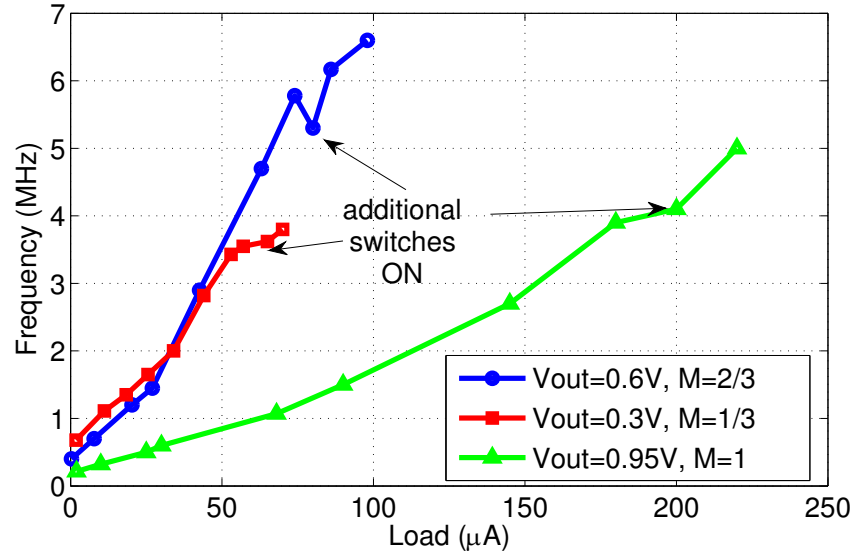


Figure 3.12 The graph shows the measurement results of the operating frequency at different output load values. These measurements are done at  $V_{out}$  of 0.3V, 0.6V and 0.95V with conversion ratios of  $\frac{1}{3}$ ,  $\frac{2}{3}$  and 1, respectively. The points at which additional switches are turned on are shown on the graph.

solution to this issue is to use different sizes for the direct switch at different conversion ratios. For a future work, we would study the possibility to make the charging through a linear regulator that would be activated by  $S_0$ , instead of a simple direct switch.

On the comparator side,  $V_{Bref}$  is chosen to be 0.1V lower than  $V_{Aref}$ . Reducing the separation between these two voltages can reduce the ripple that happens when the limits are reached, but they should not be too close to mitigate the possible impact of noise on circuit operation. In addition, since the comparator used is not a hysteresis circuit, the noise on the output voltage can trigger the comparator needlessly when the output voltage ripple is less than 14mV.

In the proposed design we have left the automation of resetting the controller to normal mode open for different strategies. In our opinion, there is no single perfect resetting strategy for all kinds of loads. Rather, each load should be studied and depending on the loading profile and the nature of the load, an appropriate resetting strategy should be designed. This is mainly to minimize the crossing of the load limits, where a significant ripple could appear. In this design, there is an apparent trade-off between area and efficiency vs regulation. To reduce the area (capacitor size) and to enhance the efficiency at very low power (using lower switching frequency), we needed to trade them off with the regulation.

Table 3.1 comparison with recently published results

Design	[40]	[45]	[43]	[29]	This work
Technology $\mu m$	0.35	0.35	0.35	0.18	0.13
Chip Area $mm^2$	7.8	N/A	$2.6 \times 2.6$	$1.6 \times 1.6$	$1.5 \times 1.5$
Active Area $mm^2$	N/A	0.48	N/A	0.57	0.52
Total On-Chip Cap.	$6.72nF$	N/A	$1.2nF$	$2.4nF$	$350pF$
On-Chip Cap. Type	3-D on chip cap	N/A	N/A	MOS Cap	Dual-MIM Cap
No. of conversion ratios	1	3	1	5	3
$V_{out}$	$0.8 - 1.5V$	$2V$	$1V$	$1.1V - 0.3V$	$1.1V - 0.3V$
$V_{in}$	$2.5V$	$15 - 5V$	$5V$	$1.2V + 1.8V$	$1.2V$
Load power range	$0.4 - 7.5mW$	$> 1mW$	$10mW$	$5\mu - 1mW$	$1 - 230\mu W$
Efficiency range	$50 - 66.7\%$	$28 - 42\%$	$62\%$	$80 - 50\%$	$80 - 30\%$
Operating frequency	200 kHz - 1 MHz	1 MHz	15 MHz	15/7.5/3.75 MHz	Asynchronous

### 3.5.2 Comparison with the latest reported results

Comparing SC DC-DC converters is a tricky issue. Since applications govern the design trade-offs of DC-DC converters, various architectures and capabilities exist in the literature. There is also no figure of merit that would determine an obvious winner in terms of performance when comparing these different architectures. Efficiency is a good comparison starting point, but keep in mind that it is very dependent on the technology, type and size of capacitors used and the test environment. Moreover, there is no unified definition of the efficiency of a SC DC-DC converter, which makes it hard in some cases to determine which energy losses were included in the measurement of efficiency. That being said, we made our best effort to compare the proposed converter with other integrated step down SC DC-DC converters that exploit a closed loop control approach.

In Table 3.1 a comparison between this work and other SC DC-DC converters found in the literature is presented. All the listed SC DC-DC converters are fully integrated except [45]. The efficiencies range from 80% to 28% for various output load conditions. It can be seen that the maximum load power that can be supplied is proportional to the size of the capacitors used. This work can provide a maximum of  $230\mu W$  because it uses only  $350pF$  and it targets ultra low power applications. In [29] a maximum efficiency of almost 80% is presented with pulsed-frequency modulation control (PFM) and automatic frequency scaling (AFM). The

AFM technique enables the converter to scale the frequency in four steps ( $15/7.5/3.75\text{MHz}$ ), but the scaling depends on a constant running clock and frequency dividers, making the design consume dynamic power even if the load is not drawing power. Note that the power consumption when there is no load is not reported for any of the competing designs. This is not the case in our proposed converter. The asynchronous drive approach will stop the switching completely if the load does not draw any power. We measured an overall power consumption of approximately  $5\mu\text{W}$  when providing output power of  $1\mu\text{W}$ . Also, the work in [29] uses two power supplies (1.2V and 1.8V) to operate the converter. For biomedical implants, this is not convenient because using additional power source (battery) requires more space. By contrast, the work in [43] uses a DPWM control approach that can apply frequency scaling through a V-to-f converter and a ring oscillator. Their design necessarily has dynamic power losses in the control circuit when the load is not drawing power and the switching frequency cannot go below 200 kHz (the frequency of the clock generator). The multiple conversion ratios technique allows our converter and the converter proposed in [29] to better utilize the voltage range provided by the supply.

### 3.6 Conclusion

In conclusion, we have presented a switched capacitor DC-DC conversion structure capable of supporting ultra-low-power systems with an adjustable output voltage while running asynchronously. The high conversion efficiency under light loading conditions makes this design particularly suitable for biomedical implants, especially if their embedded circuits apply a DVS approach to save energy. The structure uses an asynchronous controller that works as an asynchronous state machine to drive the SC converter. This asynchronous behavior reduces the dynamic power losses to the minimum and helps extending the battery life of an implant. The structure also has a mode detector that can inspect the condition of the SC network and decide whether or not additional parallel switches should be activated. In addition, The mode detector cooperates with a mode selector that can switch the system to a backup synchronous operation if the loading current exceeds the limits. This design was fabricated in  $0.13\mu\text{m}$  CMOS technology. It operates on 1.2V input voltage and produces an output voltage in the range of 300mV to 1.1V. The proposed converter can support up to  $230\mu\text{W}$  with a total of  $350\text{pF}$  on chip capacitance and is able to start up from 0V to 0.95V in less than  $408\text{ns}$ . Finally, a detailed measurement of the efficiency was provided to better understand the contributions of different kinds of losses on the design, and a comparison between this work and recent other designs was presented.

## Acknowledgments

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# Chapter 4

## Additional Circuits and Results

This chapter provides additional detailed information about the building blocks described in chapter 3, as well as additional simulation and measurement results. The information here is either a continuation or an in-depth look of what was mentioned before. A global view of the system is presented in chapter 3, which is a journal paper submitted for publication in the Transaction on Biomedical Circuits and Systems. To avoid redundancy, results that have been presented previously are not shown again here.

### 4.1 Asynchronous Controller Circuit

As mentioned in chapter 3 the Asynchronous Controller is a fully digital asynchronous state machine (ASM). What is interesting about an ASM is that it does not depend on a clock signal, but rather on external events and delays in the digital gates. By freeing the controller from the clock, the SC DC-DC converter is given the liberty to be used with any system regardless of the system's clock. Furthermore, even if a SC DC-DC converter provided its own clock, the random process variation would result in a change in that frequency. Since ASMs are driven by events, process variations do not have a significant effect on the operation of the Asynchronous Controller. In this chapter we will briefly show the steps followed to realize the proposed Asynchronous Controller.

#### 4.1.1 Synthesis of the Asynchronous Controller

In chapter 3 we have explained the behavior of the proposed asynchronous controller and the events which drive it. Then we extracted a state flow diagram that represents that behavior (as shown in Fig. 3.6). This section will continue with the process of synthesizing the Asynchronous Controller as described in section 2.4.

From that state flow diagram (Fig. 3.6), a flow table is constructed (Table 4.1). In that table, the stable states are underlined. The stability of the controller is guaranteed since each unstable state will lead to a stable one. Moreover, notice that in the case of an input of  $V_A V_B = '10'$ , the states are not defined. That is due to the fact that  $V_B$  is generated from



Table 4.1 Asynchronous Controller flow table.

Present state	Next state				Output $S_0S_1S_2$
	$V_AV_B = 00$	01	10	11	
I	<u>I</u>	<u>I</u>	-	II	100
II	I	III	-	<u>II</u>	000
III	I	<u>III</u>	-	IV	010
IV	I	V	-	<u>IV</u>	010
V	I	<u>V</u>	-	VI	001
VI	I	III	-	<u>VI</u>	001

Table 4.2 Asynchronous Controller excitation table.

Present state $y_0 y_1 y_2$	Next state				Output $S_0S_1S_2$
	$V_AV_B = 00$	01	10	11	
	$Y_0 Y_1 Y_2$	$Y_0 Y_1 Y_2$	$Y_0 Y_1 Y_2$	$Y_0 Y_1 Y_2$	
111	111	111	ddd	011	100
011	111	001	ddd	011	000
001	111	001	ddd	000	010
000	111	100	ddd	000	010
100	111	100	ddd	010	001
010	111	001	ddd	010	001

the comparator at a lower threshold than  $V_A$ , making the case of  $V_A V_B = '10'$  impossible. To transform the flow table into an excitation table, we will assign to the states *I*, *II*, *III*, *IV*, *V* and *VI* the values '111', '011', '001', '000', '100' and '010' respectively. Table shows the excitation table obtained from this step. By inspecting this table, it can be seen that the previous assignment of boolean values to the states ensures that none of the subsequent states are complements of each other. Moreover, undefined states are assigned a "don't-care" value represented by the letter 'd'.

In Fig. 4.1 the Karnaugh maps for the outputs ( $S_0$ ,  $S_1$  and  $S_2$ ) and the next state ( $Y_0$ ,  $Y_1$  and  $Y_2$ ) are extracted from Table 4.2. It is simple to obtain the boolean equations for  $S_0$ ,  $S_1$  and  $S_2$  from their Karnaugh maps. This is not the case for  $Y_0$ ,  $Y_1$  and  $Y_2$  since their Karnaugh maps are much larger. With the help of a Karnaugh map minimizer software [18] the following boolean equation are obtained:

$$\begin{aligned}
S_0 &= y_0 \cdot y_1 \cdot y_2 \\
S_1 &= \overline{y_0} \cdot \overline{y_1} \\
S_2 &= \overline{y_2} \cdot (y_0 + y_1) \\
Y_0 &= \overline{V_A} \cdot y_1 + \overline{V_A} \cdot y_2 + y_1 \cdot y_2 + \overline{V_B} \\
Y_1 &= V_A \cdot y_0 + V_A \cdot y_1 + y_0 \cdot y_1 + \overline{V_B} \\
Y_2 &= \overline{V_A} \cdot \overline{y_0} + \overline{V_A} \cdot \overline{y_1} \cdot \overline{y_2} + \overline{V_B}
\end{aligned} \tag{4.1}$$

With these equations, the Asynchronous Controller digital circuit is implemented (Fig. 4.2). Note that an additional buffering stage was added in the circuit of the Asynchronous Controller to keep the transition in the digital signals fast. This helps to reduce short-circuit currents in the logic gates and reduce the average power consumption.

## 4.2 Signal Router Circuits

The signal router block, shown in Fig. 3.3, is the circuit that delivers driving signals to the gates of the switches in the SC network (Fig. 3.2). According to signals  $T_1$  and  $T_2$ , appropriate drive signals are routed to switches ( $G_1, G_2, \dots, G_{11}$ ) providing a conversion ratio of 1,  $\frac{2}{3}$  or  $\frac{1}{3}$ . The routing is done by a group of 4-to-1 multiplexers. Since there are 11 switches in the network, 11 multiplexers are used. Table 4.3 lists the input and output of each of the multiplexers depending on the signals  $T_1$  and  $T_2$ .

In addition to choosing the conversion ratio, the signal router can turn additional switches ON when the *Support* signal is high. Recall that the *Support* signal is issued by the mode detector to increase the size of the switches when needed. In Fig. 3.3, switches controlled by  $G_2$ ,  $G_7$  and  $G_9$  consist of two sets of switches. One set does not depend on the *Support* signal, while the other does. The circuit which enables the additional switches as well as the configuration of the additional switches are shown in Fig. 4.3. Note that the enabling of these switches is done by a simple NAND gate. When the *Support* signal is low, the output ( $G_{X\_add}$ ) is low and the additional switches are OFF. On the other hand, When *Support* is high, the NAND gate will pass the drive signal ( $G_X$ ) to the additional switches.

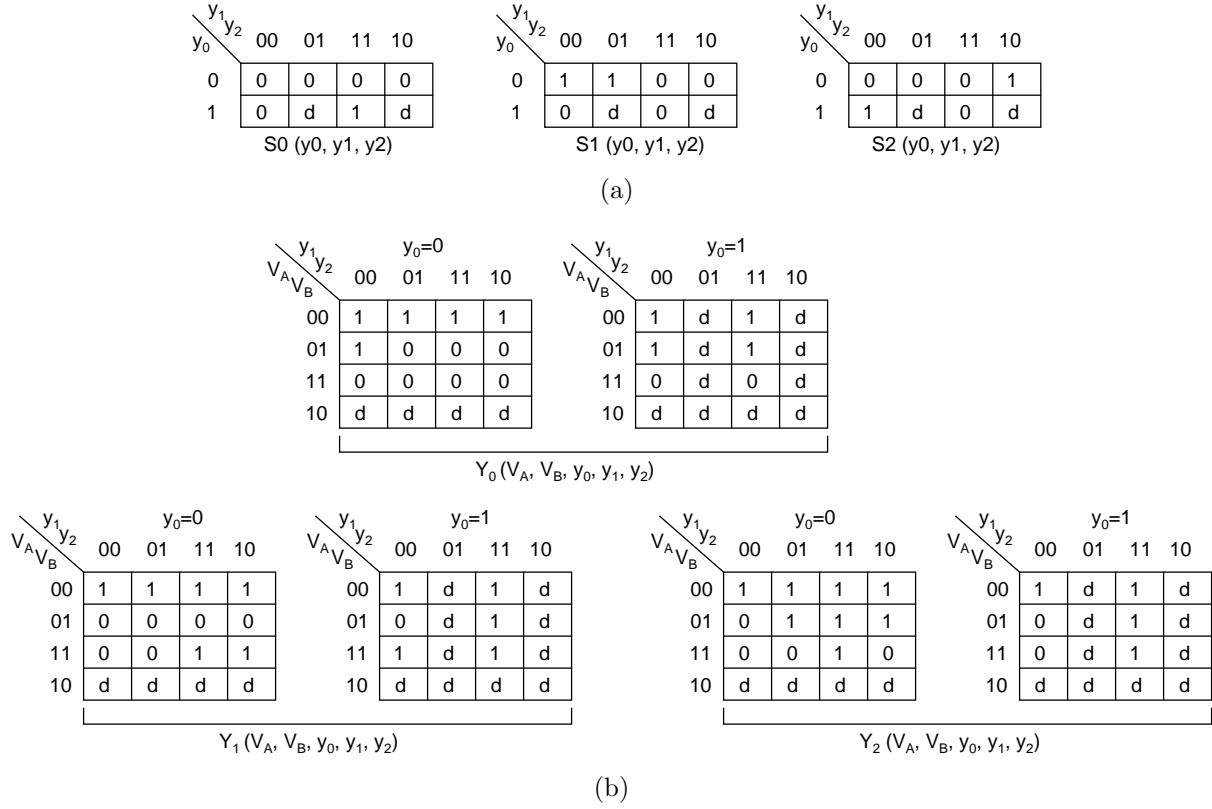


Figure 4.1 Asynchronous Controller Karnaugh maps extracted from the excitation table for: (a) the outputs ( $S_0$ ,  $S_1$  and  $S_2$ ), (b) next states ( $Y_0$ ,  $Y_1$  and  $Y_2$ ).

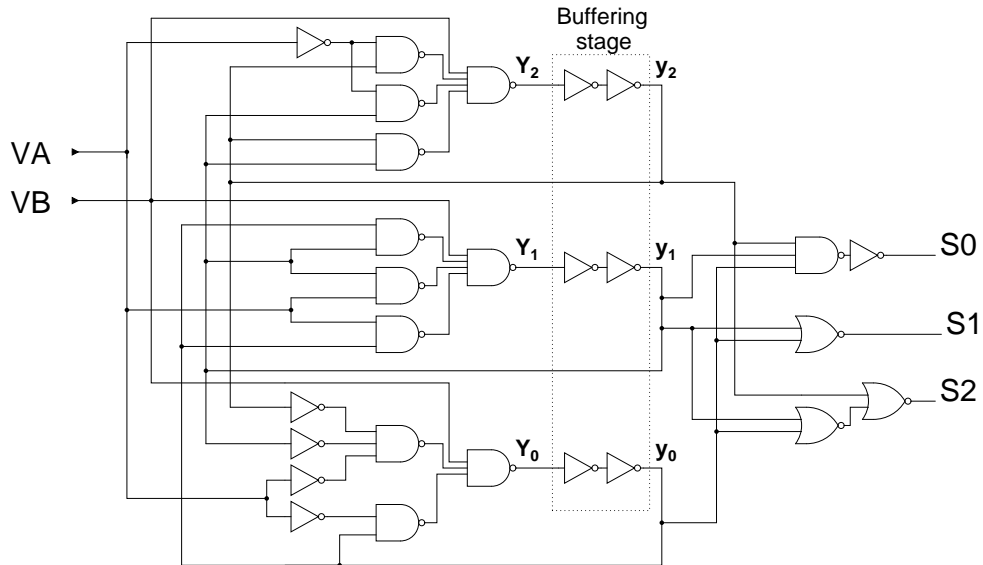


Figure 4.2 The full digital circuit of the Asynchronous Controller block that appears in Fig 3.1.

Table 4.3 The signal router's output for each switch in the SC network according to the conversion ratio needed (set by  $T_1$  and  $T_2$ ).  $\phi$  is one of the drive signals, either  $S_1$  or  $S_2$  in the Asynchronous Drive Mode, or the clock signals ( $CLK$  and  $\overline{CLK}$ ) in the Synchronous Drive Mode.

$T_1T_2$	00	01	10	11
Conversion Ratio (M)	1/3	2/3	1	Deactivated
Switch Control Signal (output of MUX)	Drive Signal (input of MUX)			
$G_1$	$\phi$	$\phi$	$\phi$	GND
$G_2$	$\overline{\phi}$	$\overline{\phi}$	$\overline{\phi}$	GND
$G_3$	$\overline{\phi}$	$\overline{\phi}$	$V_{dd}$	GND
$G_4$	$\phi$	$\phi$	GND	GND
$G_5$	GND	GND	$\phi$	GND
$G_6$	GND	$\phi$	GND	GND
$G_7$	$\overline{\phi}$	GND	$\overline{\phi}$	GND
$G_8$	$\phi$	$\overline{\phi}$	GND	GND
$G_9$	$\overline{\phi}$	$\overline{\phi}$	$\overline{\phi}$	GND
$G_{10}$	GND	GND	$\phi$	GND
$G_{11}$	$\overline{\phi}$	$\phi$	$V_{dd}$	GND

### 4.3 Mode Selector Circuits

Just like the Signal Router, the Mode Selector is based on multiplexers. However, since these signals are the drive signals, the non overlapping criteria has to be ensured. The generation of the complementary signals for  $S_1$  and  $S_2$  are done within the Mode Selector. Fig. 4.4 shows the circuits of the Mode Selector. The multiplexers output depends on the *Decision* signal. When the *Decision* signal is low, the Mode Selector will forward the signals  $S_0$ ,  $S_1$  and  $S_2$  (with their non-overlapping compliments) to the SC DC-DC converters network, putting it in Asynchronous Drive Mode. Otherwise, when the *Decision* signal is high, the Mode Selector forwards the clock signals ( $CLK$  and  $\overline{CLK}$ ) making the SC DC-DC converter operate in Synchronous Drive Mode. Notice that in the Synchronous Drive Mode the two converters inside the SC DC-DC converters network are time interleaved and the direct switch is deactivated (see Fig. 3.2).

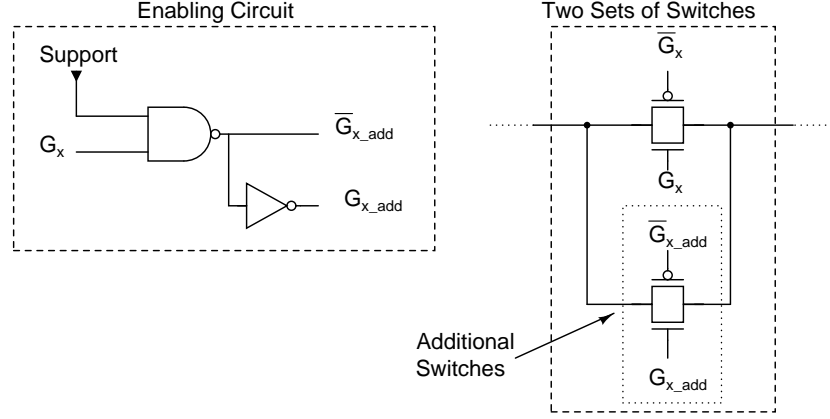


Figure 4.3 The enabling circuit within the Signal Router. When *Support* signal is low  $G_{X\_add} = GND$ . When *Support* signal is high  $G_{X\_add} = G_X$ .

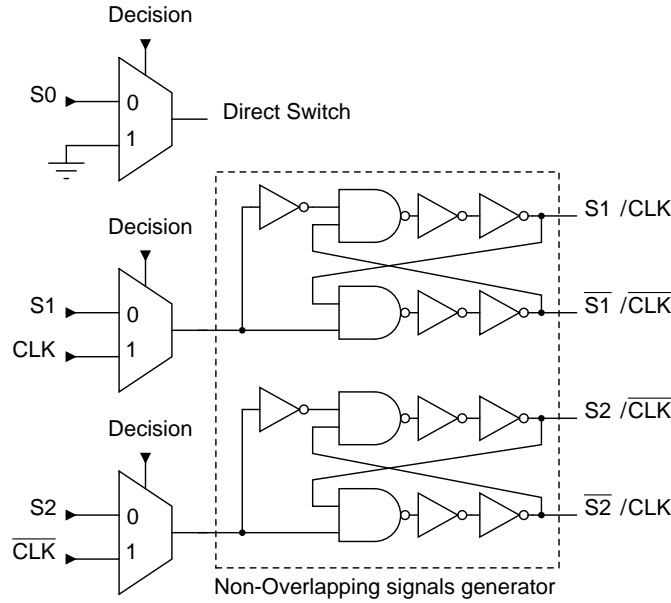


Figure 4.4 The Mode Selector circuit consisting of multiplexers and non-overlapping signal generators.

## 4.4 Dual-Threshold Comparator Design

As was shown in Fig 3.1, a dual threshold comparator is used in the structure of the converter to establish a feedback from the output to the controller. The comparator that was used for this converter is shown in Fig. 4.5. Since the operation of the controller needs two thresholds, two comparators would normally be used. However, to save on power consumption and area, we alternatively used a dual threshold comparator. The latter is based on an OTA and current mirrors. This was inspired by the work done in [16].

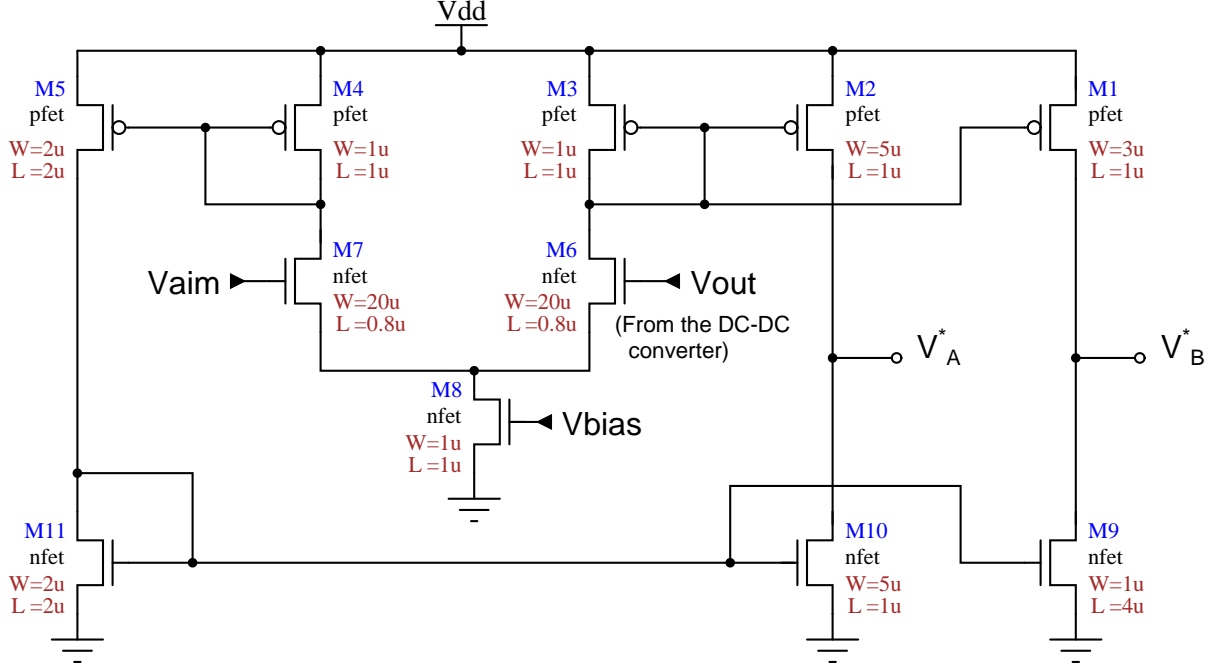


Figure 4.5 The dual threshold comparator based on OTA and 3 current mirrors.  $V_A^*$  and  $V_B^*$  are the unbuffered outputs of the comparator.

The comparator operates as follows.  $M_8$  works as a current source that biases the rest of the comparator. The differential pair  $M_6$  and  $M_7$  will take the output of the converter ( $V_{out}$ ) and compare it with the reference voltage ( $V_{aim}$ ).  $V_{aim}$  is the desired output voltage of the DC-DC converter. It can be provided by a voltage divider or a DAC. The result of the comparison will drive a current in one of the branches of the differential pair. The current is then conveyed to  $M_2$  and  $M_{10}$ . The difference between the drain currents of  $M_2$  and  $M_{10}$  will either pull up  $V_A^*$  to  $V_{dd}$  (1.2V) or sink it to ground. The transistors  $M_2$  and  $M_{10}$  are sized such that  $V_A^* = 0.6$  when  $V_{out} = V_{aim}$ . By changing the sizes of the output transistors, the threshold can be shifted.  $M_1$  and  $M_9$  are sized so that their currents will result in a threshold lower than the first one. In this design,  $V_B^*$  is produced at a threshold lower than  $V_A^*$  by 60mV. To generate  $V_A$  and  $V_B$ , which trigger the Asynchronous controller,  $V_A^*$  and  $V_B^*$  are buffered with a couple of inverters.

This comparator is still a prototype and was not fully optimized. Yet, it provides good results. Fig. 4.6 presents the DC analysis simulation results of the comparator shown in Fig. 4.5. The sweep is done with  $V_{bias} = 0.2V$  and  $V_{aim} = 0.6V$ . The results in Fig. 4.6(a) shows the generation of both  $V_A^*$  and  $V_B^*$ . The first threshold is measured at 599.2mV while the lower threshold is at 541.1mV. In post-layout simulations (PLS), the thresholds are at

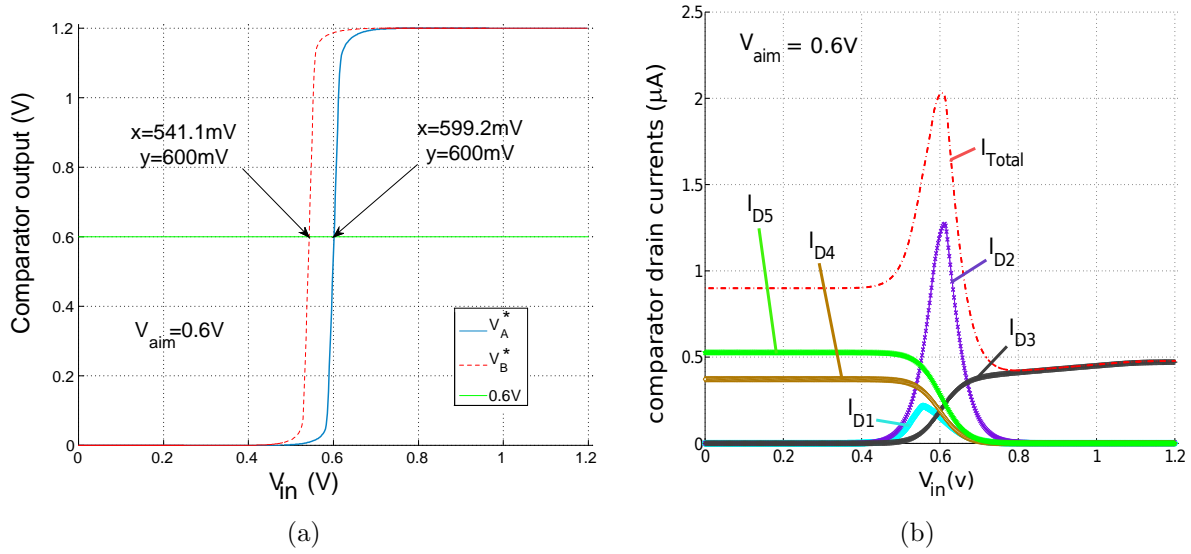


Figure 4.6 The results of the DC analysis of the comparator: (a) Show the input-outputs voltage characteristic, (b) Shows the comparator drain currents Vs input voltage characteristics.

596.3mV and 538.7mV. As for the power consumption, this comparator has a low power consumption. Fig. 4.6(b) shows the current in each branch of the comparator, as well as the total current consumed. The maximum power consumption for this comparator is 2.4 $\mu W$  and it occurs when  $V_{out} = V_{aim}$ . The measurement of the chip showed that the comparator is affected by the noise on the output when the voltage output ripple is lower than 14mV and it still needs improvements.

## 4.5 Additional Measurement Results

### 4.5.1 Transition Between Driving Modes

In this section, a brief look on the transition between the two modes of operation (ADM and SDM) is discussed. When the loading current exceeds the limits,  $V_{out}$  will drop and the pattern in the drive signals  $S_0$ ,  $S_1$  and  $S_2$  starts to change. This change is detected by the Mode Detector which issues the *Support* signal to add additional switches. If the activation of the additional switches was not enough,  $V_{out}$  will drop again making the *Decision* signal becomes high. Once the *Decision* signal is issued, the Mode Selector will switch the converter to SDM. Fig. 4.7 shows PLS of the transition from ADM to SDM along with the drive signals from the Asynchronous Controller and Mode Detector. The frequency of the clock signal used

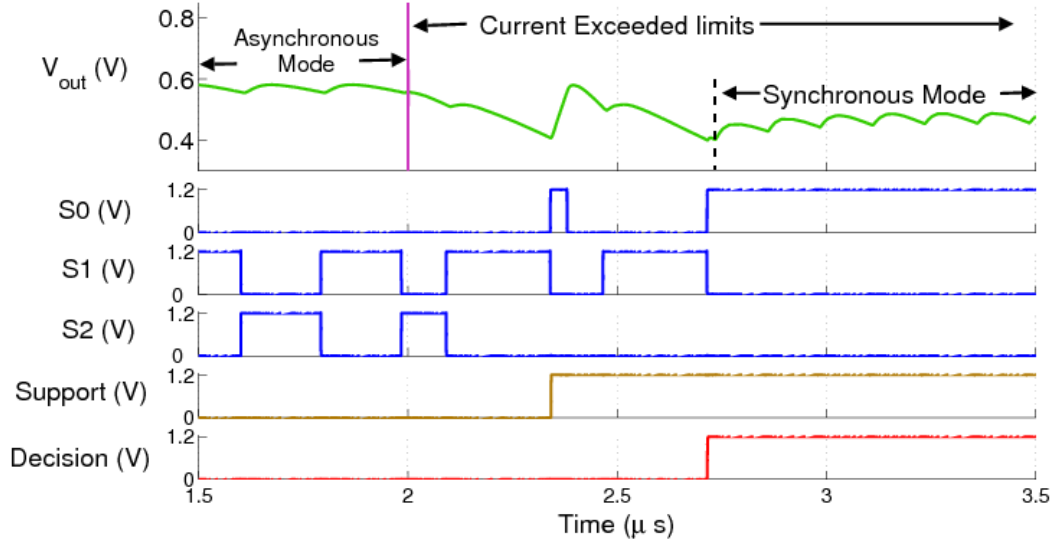


Figure 4.7 The transition from Asynchronous to Synchronous Drive Mode when the load exceeds the limit.

to drive the converters in the SDM is  $4\text{ MHz}$ .

Going back to ADM is done by resetting the Mode Detector. Issuing the Reset signal is currently manual, but can be automated in various fashions. It is better to leave the issue of resetting the Mode Detector open for the system-level designer since the best strategy for resetting the Mode Detector depends on the nature of the load. Nevertheless, one simple solution for automating the rest could be achieved by counting the pulses of the clock signals in SDM and resetting to ADM after a certain number of pulses. It is important to remember that the SDM is a back-up mode which would be rarely activated.

### 4.5.2 Additional Efficiency Results

Additional efficiency characterization in simulation, post-layout simulation and experimental measurements are shown in Figs. 4.8, 4.9 and 4.10 respectively. The effect of the parasitics can be clearly seen when comparing the figures of circuit simulation against the post-layout simulation.  $\eta_{par}$  in the simulation results almost overlaps with the  $\eta_{lin}$  at  $V_{out}$  equal to 1V and 0.6V. While in the post-layout results at the same  $V_{out}$  shows how the parasitics starts to affect  $\eta_{par}$ .

Figs. 4.10(a)-(c) are additional experimental results at output voltages other the ones previously presented in Fig. 3.10. In these figures, the voltage levels at which the efficiency



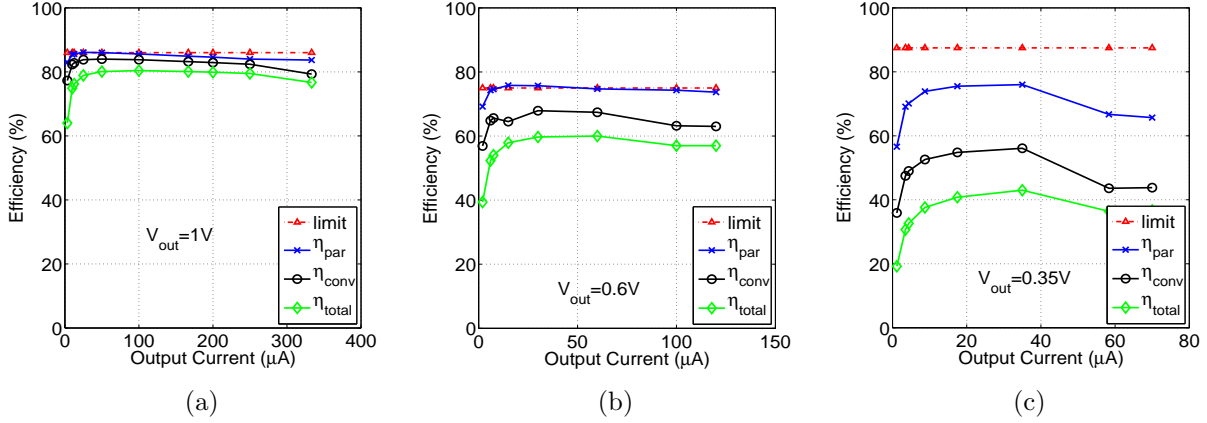


Figure 4.8 Efficiency simulation results versus the load current at (a)  $V_{out} = 1V$ , (b)  $V_{out} = 0.6V$ , (c)  $V_{out} = 0.35V$ . The three types of efficiency defined in section 3.3 are shown.

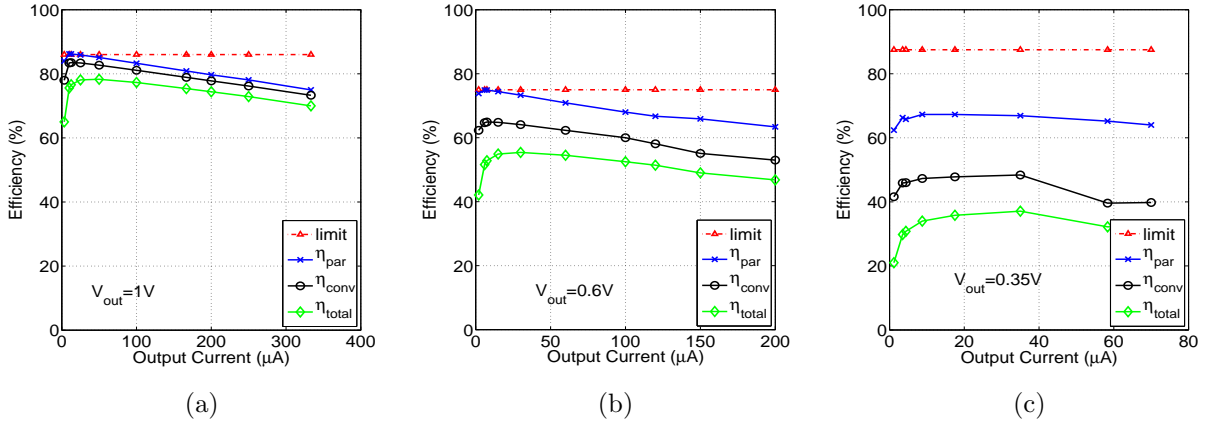


Figure 4.9 Efficiency PLS versus the load current at (a)  $V_{out} = 1V$ , (b)  $V_{out} = 0.6V$ , (c)  $V_{out} = 0.35V$ . The three types of efficiency defined in section 3.3 are shown.

was measured were very close to the no load voltage. This made the output ripple very small. In addition, the feed-through noise on the pads became significant and started to trigger the comparator, which made it almost impossible to measure the efficiency at higher loading currents. Furthermore, some part of the drop in efficiency is due to leakages in the ESD protection of the power pads. Theoretically, according to the data sheets of IBM-PDK  $0.13\mu m$  technology, these leakages should be around  $1.3\mu A$  per power pad protection circuit. Experimentally, the leakage on an ESD protection for the power pad was measured to be  $1.5\mu A$ . Since ideally this SC DC-DC converter should be implemented with other circuits on the same chip, these leakages should not be considered part of the design. Also, since the chip was designed for testing, several power pads are used, which makes the losses multiply

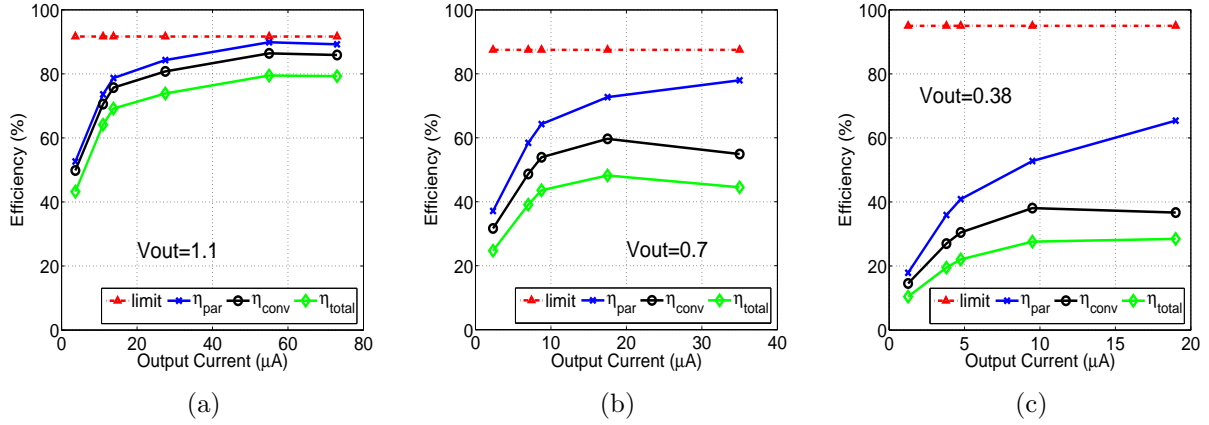


Figure 4.10 Additional efficiency experimental results versus the load current at (a)  $V_{out} = 1.1V$ , (b)  $V_{out} = 0.7V$ , (c)  $V_{out} = 0.38V$ . The three types of efficiency defined in section 3.3 are shown.

by the number of power pads (6 power pads). Nonetheless, we would like to mention that all the efficiency experimental results provided in this thesis include the losses due to leakages in only the input ESD power pad.

### 4.5.3 Additional Output Voltage Measurements

Additional output measurements in Fig. 4.11 show the settling time while the converter is loaded with a  $100pF$  capacitance and  $10k\Omega$  resistance. The converter output takes  $1.3\mu s$  to settle to  $0.35V$  and  $468ns$  to settle to  $0.64V$ . The settling time of the first case is longer due to the overshoot in the output voltage. The overshoot is a result of the large size of the direct switch and the delay in the control loop. The direct switch was sized to be able to charge the output capacitor to the highest voltage ( $1.1V$ ) at the worst case load ( $250\mu A$ ). The size selected for all the switches in the SC DC-DC converter including the direct switch is  $W/L = 50\mu m/0.5\mu m$ .

As we explained earlier in chapter 3.4, the back-up mode (Synchronous Drive Mode) is implemented to reduce the ripple in the output voltage when the load exceeds the limits. Fig. 4.12 shows that if the load exceeds the limits while the Mode Detector is deactivated, the ripple in the output voltage can be between  $0.2V$  and  $0.3V$ . Remember that exceeding the maximum current is an exceptional case that should not happen frequently.

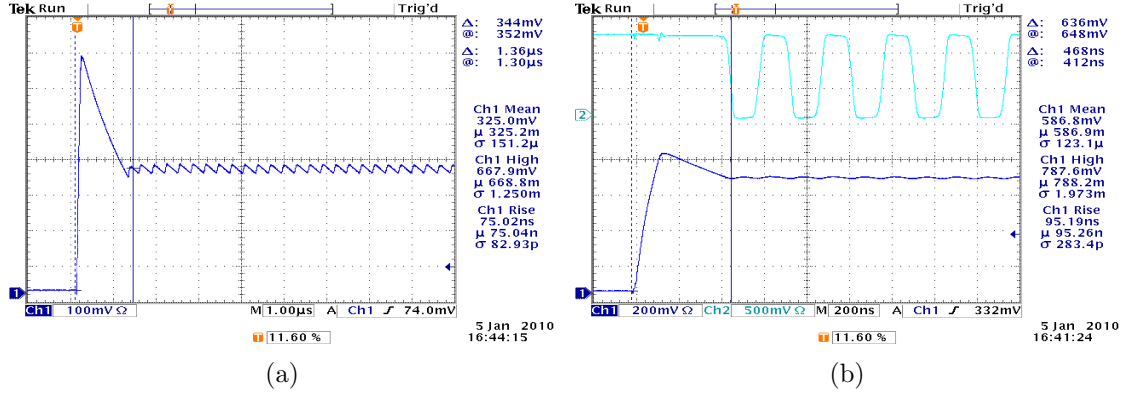


Figure 4.11 Additional measurements of the output voltage of the converter while loaded with  $10k\Omega$  and  $100pF$ : (a)  $V_{out}$  going from  $0V$  to  $0.35V$  in  $1.36\mu s$ , (b)  $V_{out}$  going from  $0V$  to  $0.64V$  in  $468ns$ .

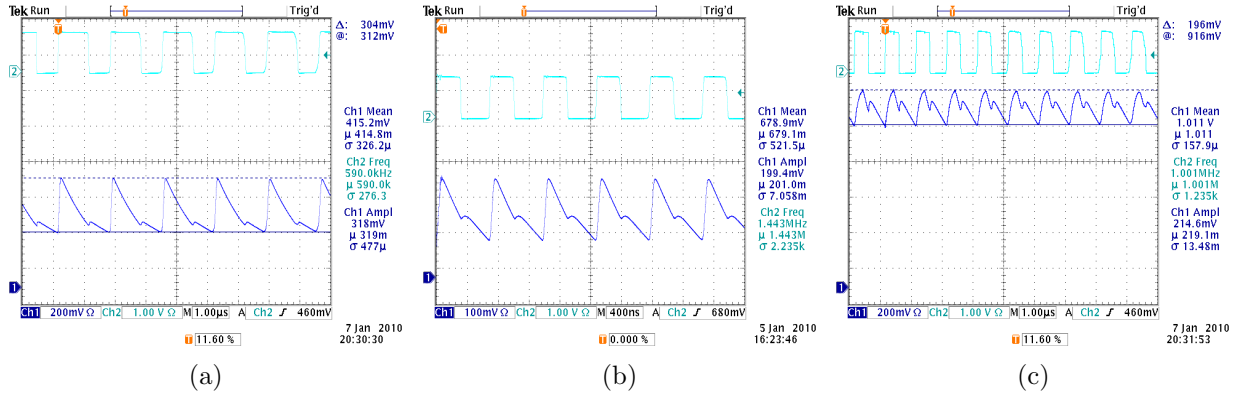


Figure 4.12 Output voltage when the load current exceeds the limits while the Mode Detector is deactivated: (a) when the converter is using a conversion ratio of  $M = 1/3$  the ripple is  $304mV$ , (b) when the converter is using a conversion ratio of  $M = 2/3$  the ripple is  $200V$ , (c) when the converter is using a conversion ratio of  $M = 1$  the ripple is  $196mV$

#### 4.5.4 Output Ripple Measurements

In the proposed design, the output voltage ripple ( $\Delta V_{out}$ ) is inversely proportional to the load current. Since the controller does not limit the overshoot of the output voltage,  $\Delta V_{out}$  can have different values according to the loading conditions. Also, as  $V_{out}$  gets lower than  $V_{NL}$ , which is the maximum output voltage for a given conversion ratio,  $\Delta V_{out}$  increases. Moreover, as in all SC DC-DC converters, the  $\Delta V_{out}$  also depends on the load capacitance. Fig. 4.13 shows the measurement of  $\Delta V_{out}$  at different conversion ratios and different output voltages. The load capacitor used for these measurements is  $100pF$  and the output ripple is in the range of  $12mV$  to  $158mV$ .

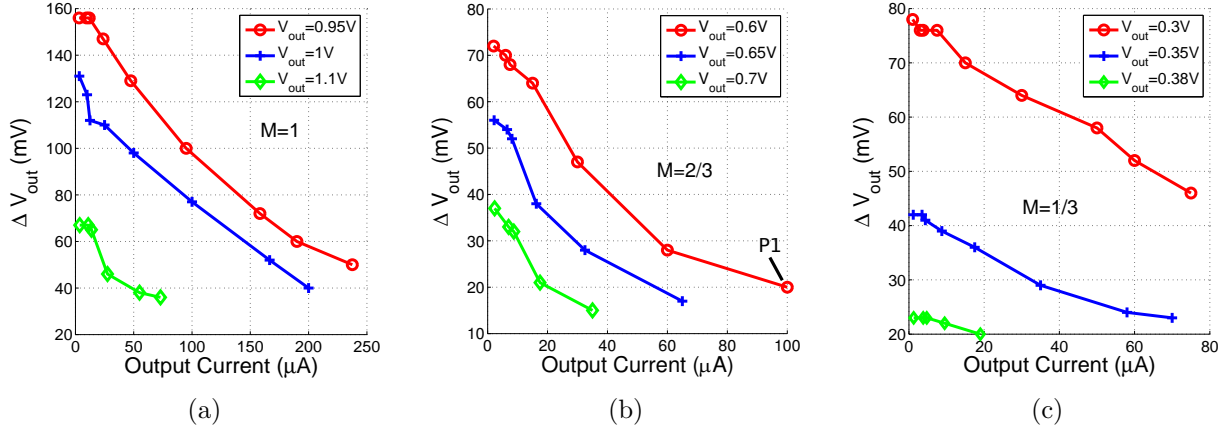


Figure 4.13 Measurement of the output voltage ripple ( $\Delta V_{out}$ ) versus the loading current at different conversion ratios ( $M$ ): (a)  $M = 1$ , (b)  $M = 2/3$ , (c)  $M = 1/3$ .

During chip testing, we observed that  $\Delta V_{out}$  becomes higher once the additional switches are ON (For example at point  $P1$  in Fig. 4.13(b)). This is because the path for charging the load capacitor has a higher resistance with smaller output switches. Hence, the rate at which the output is charged from the SC DC-DC converters is reduced, thus decreasing the overshoot (i.e. less  $\Delta V_{out}$ ). This can be considered as another advantage of adaptively sizing of the switches according to the load current.

## 4.6 Layout Precautions and Recommendations

In the process of implementing the proposed design on chip, certain layout rules were followed to ensure a fully functional chip. This section recommends important rules for layout that can protect the implemented circuits from damage or malfunction.

### 4.6.1 Layout Protective Structures

When starting the layout process, the designer should be familiar with the precaution that should be followed and the protective structures that can be used to minimize unwanted effects. The main causes for chip failures are latch-up, electromigration and floating gate effect. we will present each of these problems and the methods to avoid them. Note that the IBM CMOS  $0.13\mu m$  technology used to fabricate this design is a n-well process. This means that the wafer substrate is a p-type. Thus all the presented precautions and recommendation are for a n-well process.

**Latch-up:** One of the well-known problems with fabricated chips is latch-up. It occurs when an parasitic junction diode is forward biased and it changes the expected behavior of CMOS transistors. To avoid this problem on the schematic level of the circuit design, the bulk of a NMOS transistor is always connected to the lowest possible voltage, while the bulk of a PMOS transistor is connected to the highest voltage. Throughout this section we will assume that the lowest voltage possible is the ground ( $GND$ ) while the highest is  $V_{DD}$ . On the layout level, a substrate contact ( $p^+$ -well over substrate) is used to form the bulk connection of a NMOS transistor while a n-well contact ( $n^+$ -well over n-well) is used to form the bulk of a PMOS transistor. As in the schematic design, the bulk of a NMOS is connected to  $GND$  while the bulk of a PMOS is connected to  $V_{DD}$ . To pass a design rule check (DRC) for the layout, one bulk connection near each transistor is sufficient. However, this does not guarantee that latch-up will not occur. The best way to guard against latch-up is to surround the transistor with the bulk; this forms what is known as a guard-ring. For a NMOS, this means a substrate contact will be built around it while keeping a small gap to pass connections to the gate, drain and source of the transistor. This guard-ring will ensure that the substrate around the NMOS transistor is kept at  $GND$ . In the case of PMOS, a double guard-ring will be built. One guard-ring will be formed inside the n-well of the PMOS transistor (using n-well contacts) and connected to  $V_{DD}$ . This prevents the parasitic junction diodes inside the PMOS from activating. The other guard-ring is a substrate contact that is built around the n-well of the PMOS and is connected to  $GND$ . This makes the parasitic diode between the n-well of a PMOS and the substrate reverse biased.

**Electromigration:** Nowadays, the technology used to fabricate CMOS circuits uses very thin wires of metal to build the internal connections between circuits. As a result, the designer should be careful of how much current is going through these wires. Overloading thin wires with current causes metal electromigration. This effect results in metal deformation and changes the conductor dimensions. This creates spots of higher resistance in the wires which can cause the circuit to fail. It can also make metals next to each other fuse together creating short-circuit connections. To avoid electromigration, wires should be sized according to metal migration current density threshold and the expected current going through them. The metal migration current density threshold can be found in the documentation of the process. Taking a 10% additional safety margin is recommended in this case.

**Floating gate effect:** Implementing CMOS circuit on a silicon wafer is done through many stages [4]. During these stages, it is necessary to protect the circuit component from damage. Stages like reactive ion etching (RIE) or plasma deposition can accumulate charge

on transistor gates and capacitors. The oxide used in these part of the circuit is very thin and will break if enough potential is built around it. Damage to the gate oxide leads to shifts in the threshold voltage of a transistor and can have drastic effects on the fabricated circuits. The thin oxide can be protected by providing an alternative discharge path for the accumulated charge. The discharge path is created with an inversely connected diode between the gate or capacitance plate and the substrate. This diode is known as a tie-down diode. At wafer processing temperatures, the tie-down diode is sufficiently conductive to prevent charge up, while at normal temperatures it is considered as an open-circuit. Notice that in an NMOS transistors, the drain or source can be considered as a tie-down diode since they are built as a  $n^+$ -well over the substrate. Thus, connecting a gate to a drain/source of a NMOS transistor is enough to protect against floating gate effects. Using tie-down diodes are also recommended for pads and n-wells.

# Chapter 5

## General Discussion

This chapter provides a general discussion about the results of this master thesis. Also, it includes an analysis of the advantages and drawbacks of the proposed design. We have implemented a fully-integrated SC DC-DC converter with an asynchronous control that regulates an output voltage within a range of  $0.3V$  to  $1.1V$  from an input voltage of  $1.2V$ . By adjusting the operating frequency according to the loading conditions, the proposed converter is able to enhance the overall conversion efficiency by minimizing the switching and control energy losses. Using adjustable conversion ratios, the converter maintains good efficiency at low output voltages and reduces the output ripple. Further enhancement of the conversion efficiency at light loads is done by using an adjustable switch sizes in the SC DC-DC converter. This adjustment of the switch sizes is done using a circuit that detects the change in the pattern of the signals of the asynchronous control. Finally, to ensure robustness of the converter under unexpected loading conditions, the converter is equipped with a backup synchronous mode.

Maximizing the conversion efficiency at a low voltage range while minimizing the area of the design is the top priority of this work. This drove us to minimize the switching frequencies and the size of the capacitors used leading to an increase in the output ripple. Hence, in this work, we traded a better efficiency and lower implementation area for an increase in the output ripple.

The efficiency figures (Figs. 3.10, 4.8, 4.9 and 4.10 ) that were presented in chapters 3 and 4 show that the overall conversion efficiency achieved by the converter over a range of  $1\mu W$  to  $230\mu W$  of load power and a range of  $0.3V$  to  $1.1V$  of output voltage is between 30% to 80%. Although an efficiency of 30% might seem low, the level of power lost is small because the output power in that case is very low. From these figures, we can also see the advantages of the adopted asynchronous control. By reducing the drive signal frequency as the load decreases, the switching losses are minimized and the efficiency is improved. Moreover, due to the asynchronous nature of the control, the power consumed by the controller circuit also scales with the load. Note that the power consumed by the controller cannot reduce indefinitely, but rather it will reach a minimum when the switching stops, which is the static

power consumption of the controller.

Unfortunately, this reduction of the operating frequency to enhance the efficiency leads to an increase in the output voltage ripple. By operating the output voltage near the maximum output voltage of a topology, the ripple can be reduced. Thus, one solution to reduce the output voltage ripple is to use more conversion ratios. Of course, this will also lead to a more complex design. Moreover, in section 4.5.4 of this thesis, we presented the relationship between the output voltage ripple and the load. One of the conclusions of that section was that the output voltage ripple can be reduced by using smaller switches at light loads. This is an attractive method since it also enhances the efficiency of the converter. Another solution for loads that are very sensitive to voltage ripple is to add a low dropout regulator (LDO) between the load and the SC DC-DC converter [6, 32]. The disadvantage of this solution is the additional power consumed by the LDO. The value of the capacitance used in the converter can also affect the output ripple. Using a bigger output capacitor reduces the output ripple. This is not very convenient in our case because we are trying to minimize the area occupied by the converter.

Charging the output capacitor at start-up is done through the direct switch (shown in Fig. 3.2). This gave the converter a fast transient response when going from a lower voltage to a higher one. The direct switch was sized to be able to charge the output capacitor to the highest voltage ( $1.1\text{ V}$ ) at the worst case load ( $250\text{ }\mu\text{A}$ ). This choice leads to a bigger initial overshoot when charging at lower output voltages. A better approach is to adjust the size of the direct switch according to the conversion ratio. By having a smaller size for the direct switch at lower voltages, the overshoot that is seen in Figs. 4.11 and 4.12 can be reduced.

In general, there are additional advantages to the adopted asynchronous control. Firstly, since the controller is not based on a constant running clock, its power consumption scales proportionally with the load. Secondly, since the controller is driven by events rather than by a clock, it is more robust to process variations. Meaning that the frequency of the drive signals will be adapted automatically to any process variation affecting the sizes of capacitors or switches. Moreover, the designer does not have to manually search for the appropriate operating frequency for the selected sizes of capacitors and switches. Instead, the sizes of the components will be based only on the maximum load and output ripple targeted. Thirdly, unlike other clock based controls, the asynchronous control does not limit itself to a maximum nor a minimum frequency. Note that the minimum frequency is zero, and the maximum frequency depends of the size of the components of the converter and the topology



used. On the other hand, the main disadvantage of the proposed control method is that it does not limit the output voltage ripple.

# Chapter 6

## Conclusion

The importance of low-power circuit techniques in portable devices and biomedical implants drove researchers to develop new design methods of reducing the power consumption of these devices. Dynamic voltage scaling (DVS) is one of the famous methods of reducing power consumption of CMOS circuitry. To apply this technique, DC-DC converters with adjustable output voltage are used. For that purpose, we have designed a SC DC-DC converter that is appropriate for such applications.

One of the challenges that faces SC DC-DC converters is the low conversion efficiency at light loads. In this work, we have demonstrated an approach for efficient power delivery in ultra-low-power devices using SC DC-DC converters. One of the criteria for efficient power delivery in SC DC-DC converters under light loads is the adjustment of the switching frequency according to the loading conditions. By switching only when required, a SC DC-DC converter reduces the switching power losses. In contrast to the methods that were developed previously in this field, we proposed an asynchronous control strategy that would not only minimize the switching power losses, but also free the converter from its dependence on a constant frequency clock, and thus reduce the dynamic power losses in the controller. A special structure of SC DC-DC converters was built to match this control method.

To apply the DVS technique, the converter should be able to change the output voltage as needed. After reviewing the basics of the SC DC-DC converters, we have shown that a SC DC-DC converter should use different conversion ratios under different output voltages to maximize the conversion efficiency. The proposed design used three different topologies to realize three different conversion ratios. On the other hand, to further reduce the switching power loss in the converter, a smart detection technique was developed to adjust the size of the switches according to the load current. The developed technique, applied in the Mode Detector block, was shown to be very flexible and simple. Additionally, the adaptive sizing of the switches has also helped to reduce the output ripple of the proposed converter.

To make the converter more robust, we included a backup mode. If the load current, for any reason, exceeded the designed limits, the Mode Selector block will switch the converter

to synchronous operation. In this mode, a clock generator is enabled to drive the converter. The detection process of exceeding the maximum current is done by the Mode Detector.

Moreover, design details and results were provided for each block of the structure. The digital circuit for the asynchronous controller along with the state flow diagram and the state table were presented. The Mode Detector and the Mode Selector were explained and demonstrated to be functional in switching the converter from the Asynchronous Drive Mode (ADM) to the Synchronous Drive Mode (SDM). Finally, the design and analysis of a low power dual-threshold comparator suitable for this converter was provided.

## 6.1 Achieved Results

In this thesis, we have designed and demonstrated a fully-integrated SC DC-DC converter structure capable of supporting ultra-low-power systems with an adjustable output voltage while running asynchronously. This design was implemented in  $0.13\mu m$  CMOS technology. It occupied an area of  $0.52mm^2$  including the on-chip MIM-capacitors. The structure with the pads and ESD protections was fabricated on a  $1.5 \times 1.5mm^2$  chip. The clock generator, however, was not included in the chip. A total of  $350pF$  on chip capacitance was used to achieve an maximum output current of  $240\mu A$ . The maximum output current can be increased by increasing the sizes of the capacitors. The proposed converter was able to produce an output voltage in the range of  $300mV$  to  $1.1V$  with an input power supply of  $1.2V$ . The maximum efficiency measure under different loads and output voltages ranges from 80 to 30%. The proposed converter features a fast transient response and a reasonable output voltage ripple under various output voltages.

## 6.2 Limitations and Future Improvements

The proposed converter still has room for improvements. The comparator presented in this work suffered from issues with noise when the chip was tested. As the output voltage reaches the maximum voltage of the converter at a given conversion ratio, the output ripple decreases and the noise starts to dominate. High peaks of noise start to trigger the comparator, which leads to unnecessary switching and irregularities in the operating frequency. This could be avoided by adopting a hysteresis comparator approach.

Moreover, in this work, we have demonstrated the effect of increasing the size of switches on demand. This was done by dividing the output switches to only two sets, where one of

these sets can be enabled or disabled. The efficiency and output voltage ripple at extremely light loads can be enhanced if the output switches were divided into more than two sets. Likewise, a similar approach could be adopted for the direct switch to reduce the overshoot at start up.

Finally, some aspects of this converter can be improved by being automated. As mentioned earlier in chapter 3, going back from Synchronous Drive Mode (SDM) to the Asynchronous Drive Mode (ADM) is done by resetting the Mode Detector. This is currently done manually but can be automated in various ways. One method is by adding a counter that counts a number of clock pulse generated then reset the Mode Detector. Additionally, the setting of the conversion ratio can also be automated with the use of analog to digital converters (ADCs). Depending on the value of  $V_{aim}$ , a digital circuit can be constructed to set the values of  $T_1$  and  $T_2$ .

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# Appendix A

## Derivation Of The Linear Efficiency of SC DC-DC converters

An interesting information can be obtained when trying to calculate the efficiency of charging a capacitor from a DC supply. The circuit shown in Fig. A.1 helps to visualize the following calculations. When a capacitor with a capacitance  $C$  is charge to a voltage  $V_{in}$ , the amount of charge ( $Q$ ) on the capacitor is given by the famous equation:

$$Q = C \cdot V_{in} \quad (\text{A.1})$$

The energy on a parallel plate capacitor is defined as:

$$dE_{cap} = V_{in} dq = \frac{q}{C} dq \quad (\text{A.2})$$

$$E_{cap} = \int_0^Q \frac{q}{C} dq = \frac{Q^2}{2C} \quad (\text{A.3})$$

$$E_{cap} = \frac{1}{2} C \cdot V_{in}^2 \quad (\text{A.4})$$

On the other hand, the energy that is supplied by the power source is:

$$E_{supply} = Q \cdot V_{in} = C \cdot V_{in}^2 \quad (\text{A.5})$$

From the equation A.4 and A.5, the efficiency of charging a capacitor from a DC supply is:

$$\eta = \frac{\frac{1}{2} C \cdot V_{in}^2}{C \cdot V_{in}^2} \times 100 = 50\% \quad (\text{A.6})$$

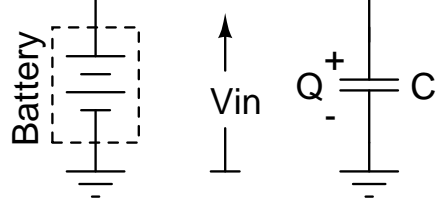


Figure A.1 Charging a capacitor from a DC supply (e.g. battery)

Notice here that capacitor stores only half of the energy supplied to it, regardless of the resistance of the charging path. The result would be the same if a resistor was included in the circuit, since this would not prevent the capacitor from accumulating the same charge, and thus, the energy stored is the same.

In SC DC-DC converters, the capacitor is partially charged and discharged. Assuming that the capacitor is charged to a voltage level of  $V_{max}$  and then discharged a voltage level of  $V_{min}$ . The energy supplied by the power source in this case is:

$$\Delta E_{supply} = \Delta Q \cdot V_{in} = C(V_{max} - V_{min}) \cdot V_{in} \quad (A.7)$$

where as the part of that supply's energy that is stored by the capacitor is:

$$\Delta E_{cap} = \frac{1}{2}C \cdot V_{max}^2 - \frac{1}{2}C \cdot V_{min}^2 = \frac{1}{2}C(V_{max}^2 - V_{min}^2) \quad (A.8)$$

From equation A.7 and A.8 the efficiency becomes

$$\begin{aligned} \eta &= \frac{\frac{1}{2}C(V_{max}^2 - V_{min}^2)}{C(V_{max} - V_{min})V_{in}} \times 100 \\ &= \frac{(V_{max} + V_{min})/2}{V_{in}} \times 100 \\ &= \frac{V_{out-avg}}{V_{in}} \times 100 \end{aligned} \quad (A.9)$$

Therefore, from equation A.9, the efficiency of a SC DC-DC converter depends only on average value of the output voltage over the input voltage. Again, the resistance of the charging path does not contribute to efficiency of the conversion.

To derive the efficiency of the SC DC-DC converter in Fig. 2.1 we define  $V_{out-max}$  as the maximum output voltage that each of the two capacitors acquire before connecting in parallel with the load. Where as  $V_{out-min}$  is the minimum output voltage that each the two capacitors discharge to before connecting back in series with the source. In this case, the energy supplied by the source is:

$$\Delta E_{supply} = \Delta Q \cdot V_{in} = \frac{C}{2}(2V_{out-max} - 2V_{out-min}) \cdot V_{in} = C(V_{out-max} - V_{out-min}) \cdot V_{in} \quad (A.10)$$

and the energy acquired in each capacitor (or the energy delivered to the load from each capacitor) is:

$$\Delta E_{cap} = \frac{1}{2}C \cdot V_{out-max}^2 - \frac{1}{2}C \cdot V_{out-min}^2 = \frac{1}{2}C(V_{out-max}^2 - V_{out-min}^2) \quad (A.11)$$

From equation A.10 and A.11 the efficiency of a two capacitor series-parallel SC DC-DC converter is the following:

$$\begin{aligned} \eta &= \frac{2 \times (\frac{1}{2}C(V_{out-max}^2 - V_{out-min}^2))}{C(V_{out-max} - V_{out-min})V_{in}} \times 100 \\ &= \frac{(V_{out-max} + V_{out-min})}{V_{in}} \times 100 \\ &= 2 \times \frac{V_{out-avg}}{V_{in}} \times 100 \end{aligned} \quad (A.12)$$

where  $V_{out-avg} \leq V_{in}/2$ . Comparing equation A.9 and A.12, we find that the efficiency of this converter was multiplied by a factor of 2. This term appeared in the equation because the topology of the converter in Fig. 2.1 has a conversion ratio of  $M = \frac{1}{2}$ . The result of the last equation can be generalized for any SC DC-DC converter with a conversion ratio  $M$ :

$$\eta_{lin} = \frac{1}{M} \frac{V_{out}}{V_{in}} \quad (A.13)$$

This term of efficiency is called the linear efficiency and is considered as the maximum efficiency that a SC DC-DC converter can have for a given  $V_{out}$ ,  $V_{in}$  and a conversion ratio  $M$  [21, 29].